Towards General Rely-Guarantee Reasoning for Concurrent, Value-Dependent Noninterference

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Confidentiality (Information Flow) Proofs

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seL4 (Murray et al., S&P 2013)

- General intransitive noninterference over functional spec, transferred to C code by refinement; binary by TV
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mCertiKOS (Costanzo et al., PLDI 2016)

- Strict noninterference between user processes over functional spec, transferred to binary via CompCert
- mCertiKOS: process creation, page fault handling, cooperative scheduling; no IPC
- approx 3,000 C SLOC and (unlike seL4) ~350 asm

Kernel-Only vs Whole-System

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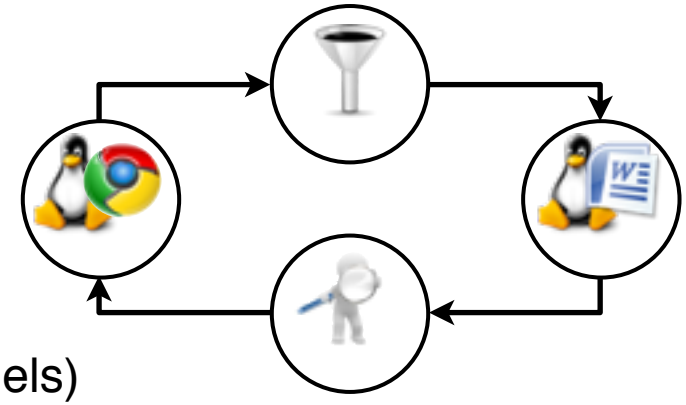
Kernel-Only Confidentiality

- assumes all application components are maximally hostile
- proved security only by reasoning about kernel enforced abstractions
  - no concurrency (for single-threaded kernels)
- simple static policies only



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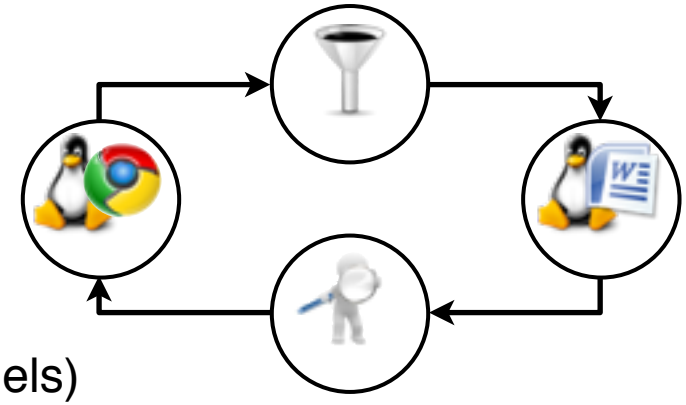
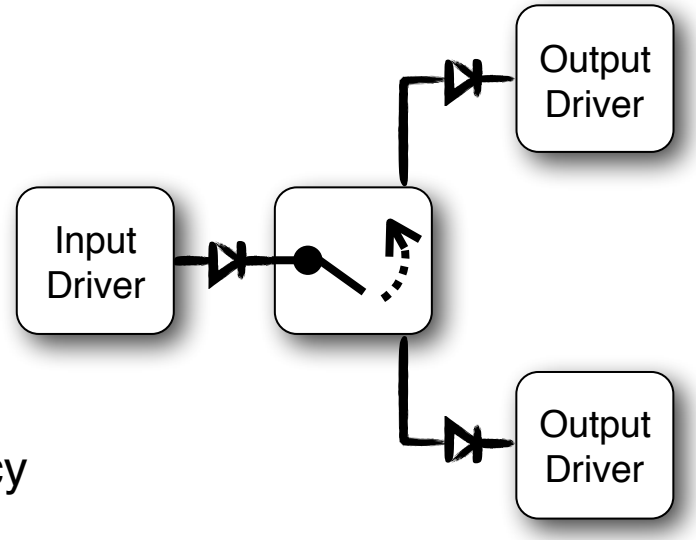


Whole-System Confidentiality

- reasons about behaviour of application components
- proves that their composition yields a secure system
  - time to start worrying about concurrency



The Cross Domain Desktop Compositor

Australian Government

Department of Defence

Defence Science and Technology Group

Mark Beaumont

CDC

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DATA 61

CSIRO

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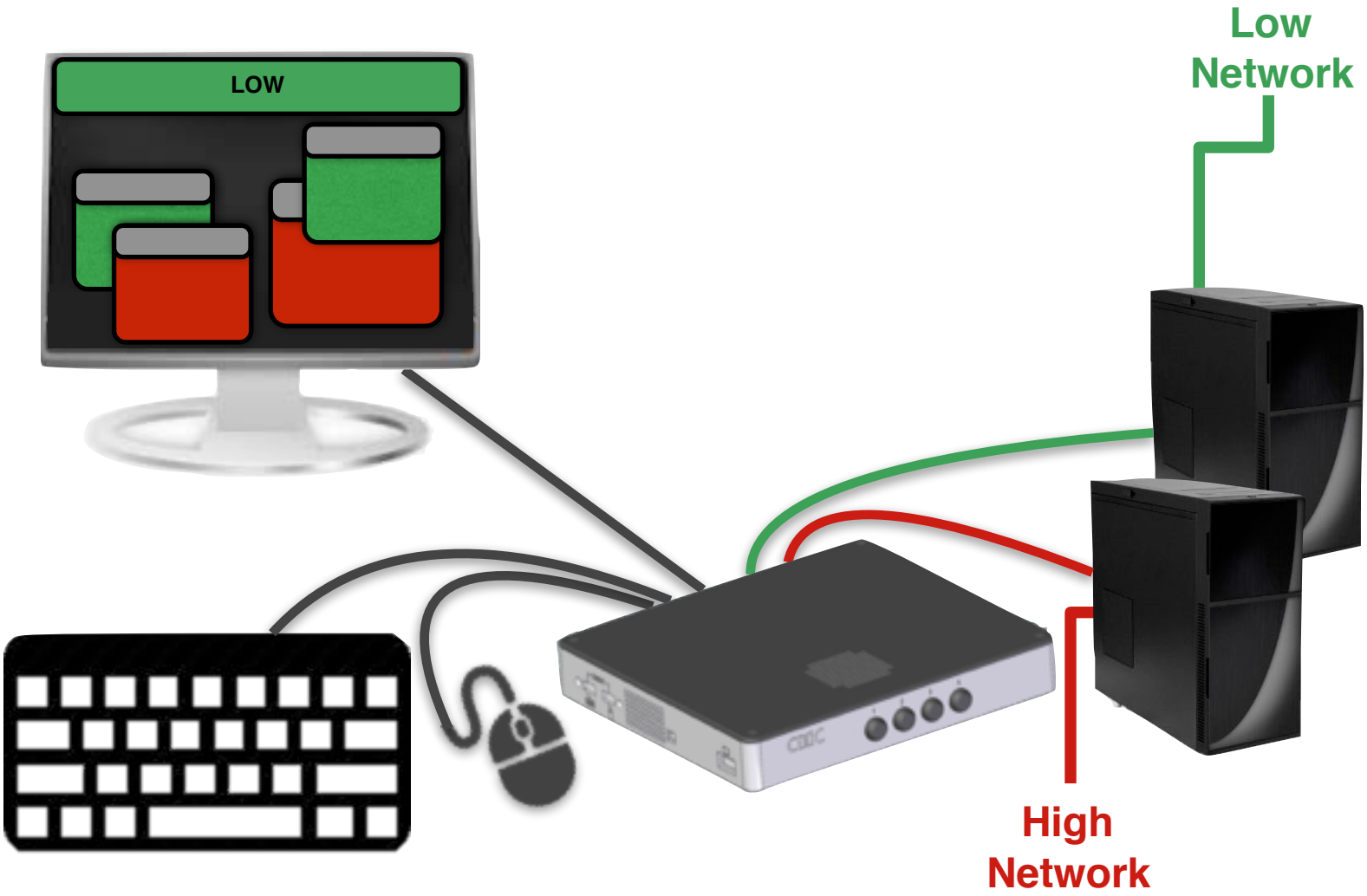

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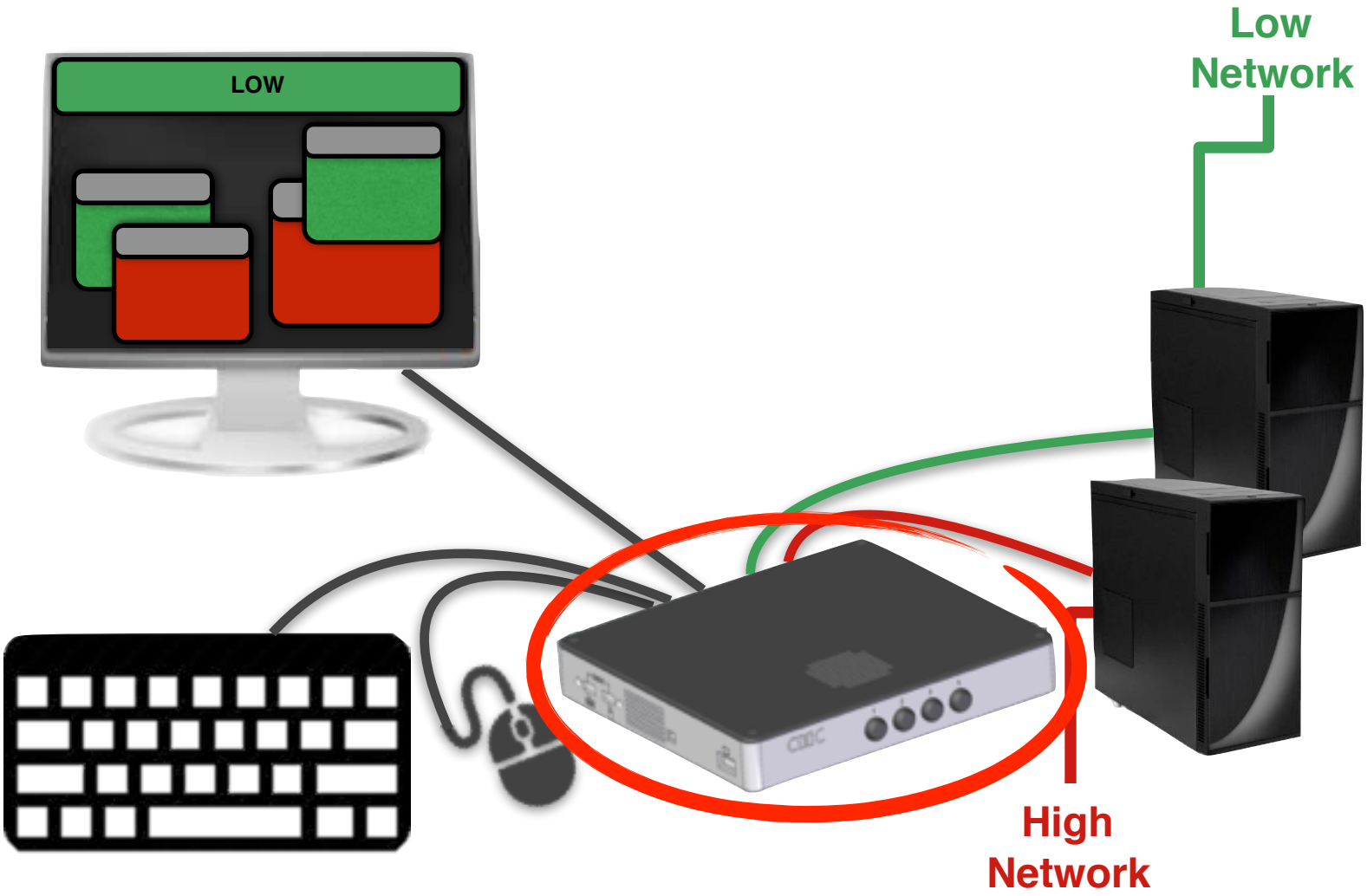
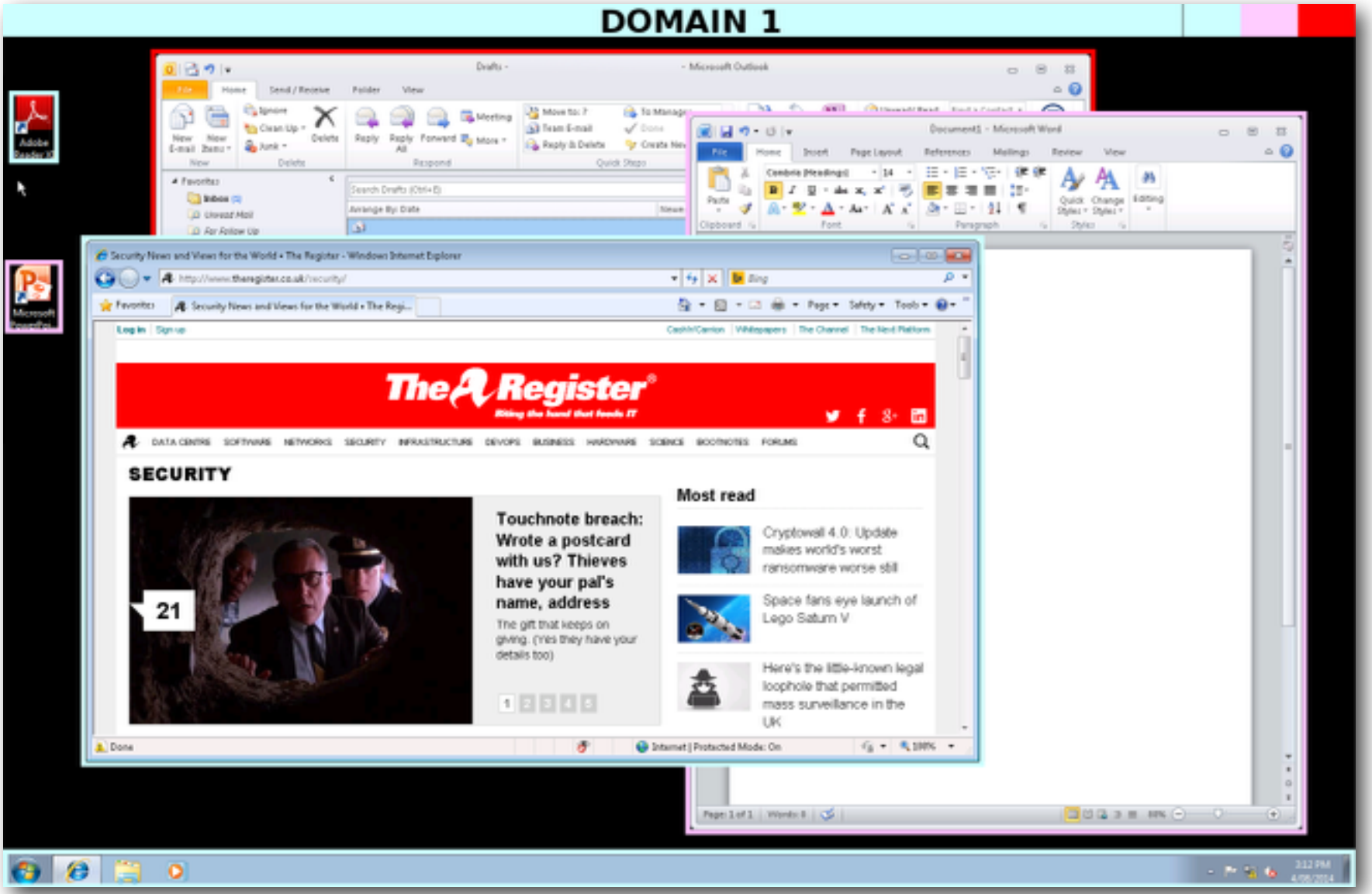
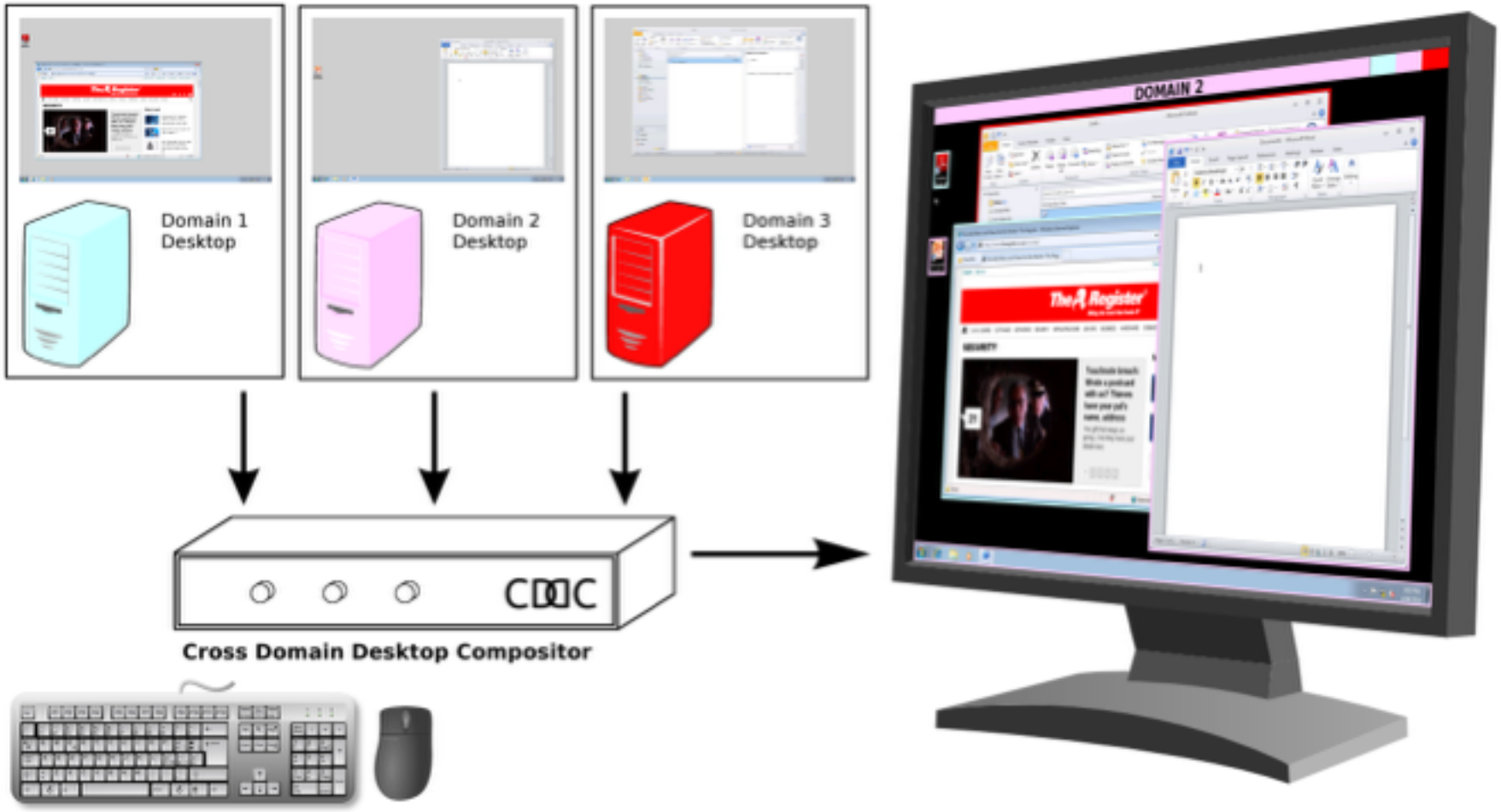


CDDC

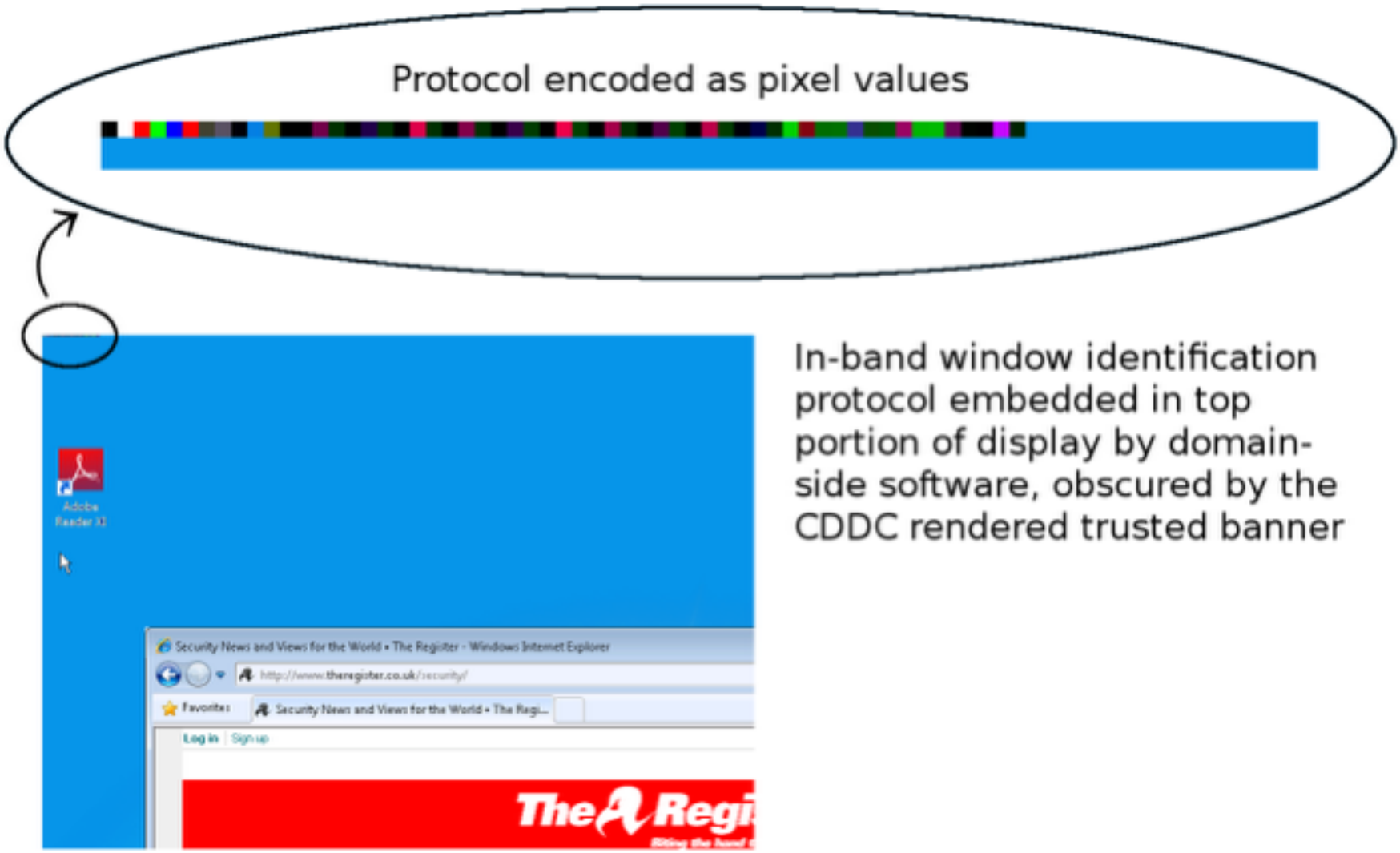
CDDC User Experience



Display Composition

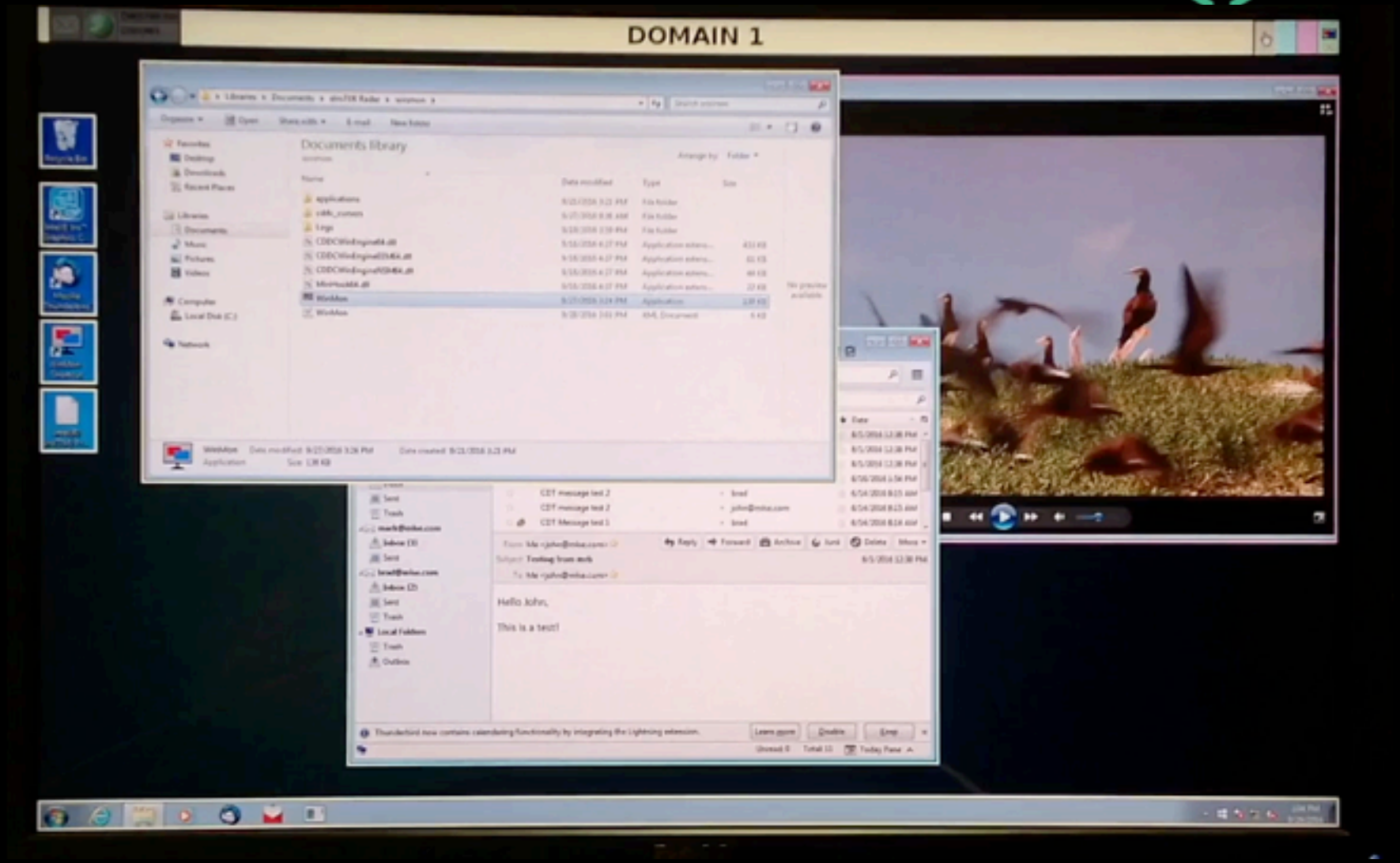


In-Band Composition Protocol



In-band window identification protocol embedded in top portion of display by domain-side software, obscured by the CDDC rendered trusted banner

Demo



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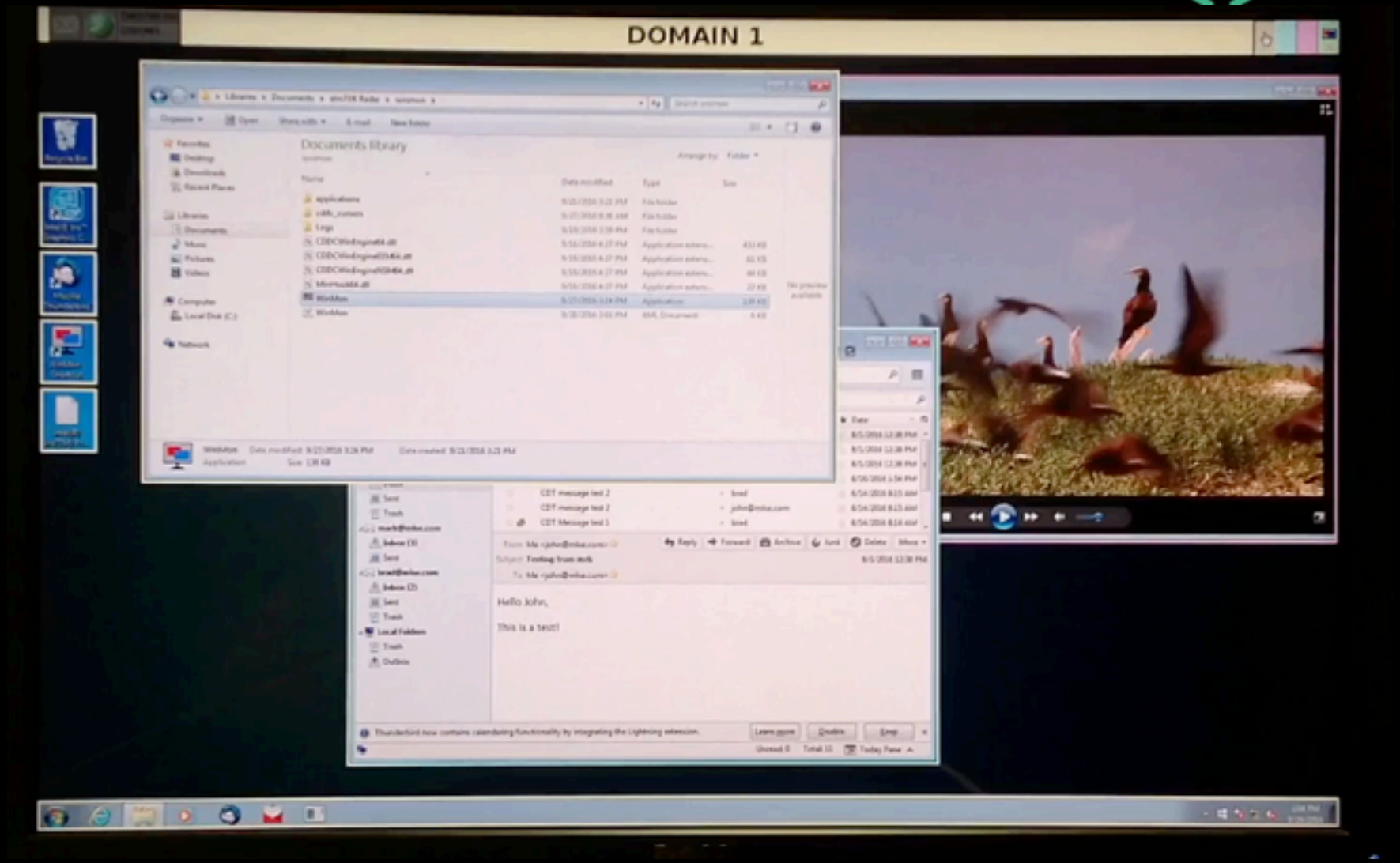

CDDC Functionality

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Video Compositing

- Very high bandwidth
- Fixed protocol and policy

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Input Processing

- Low bandwidth
- Policy dependent
  - mouse hover passthrough
  - keyboard shortcut domain switching
  - keystroke broadcast (e.g. Windows-D)
- Runtime configuration dependent
  - keyboard shortcuts for trusted path actions

CDDC Architecture

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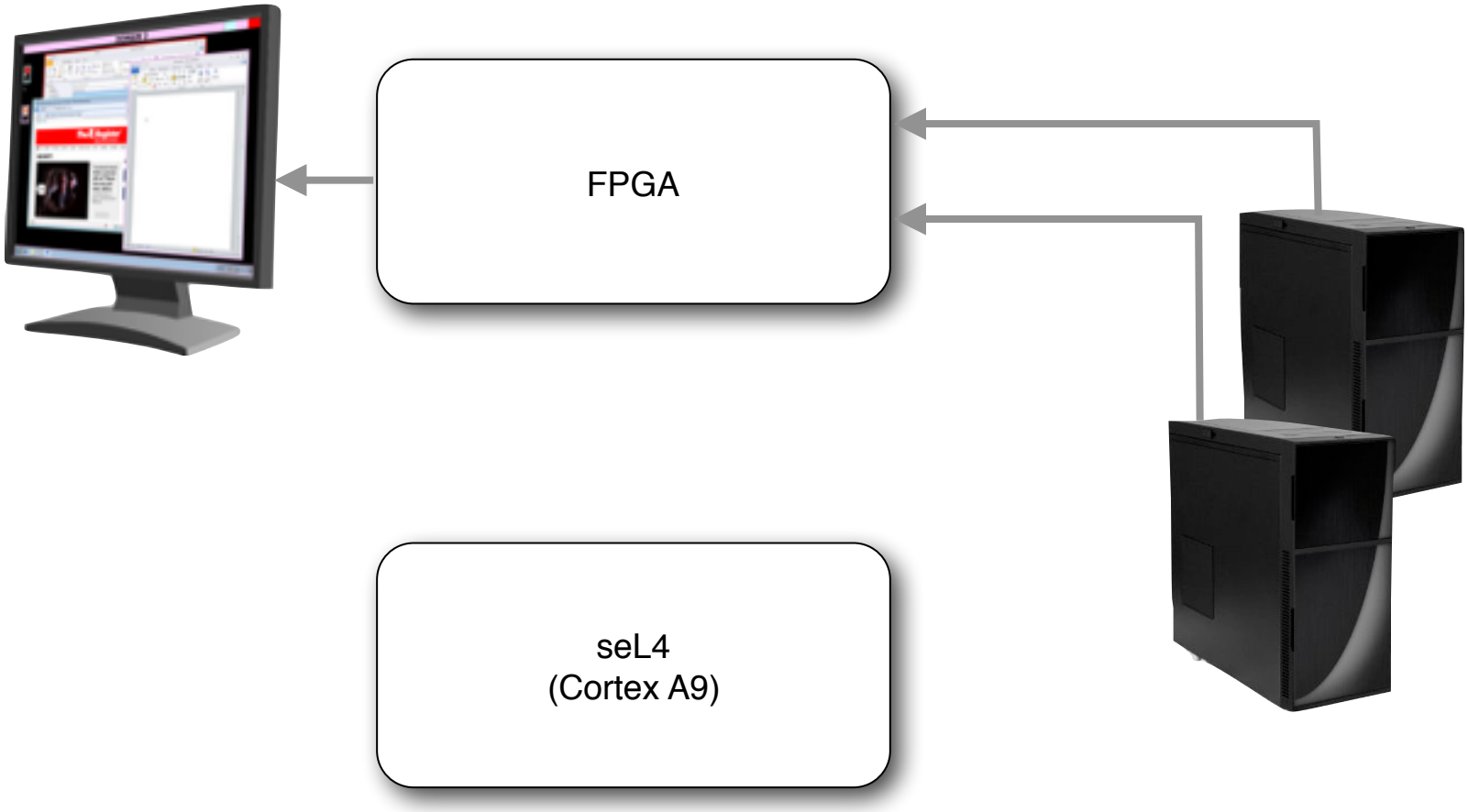

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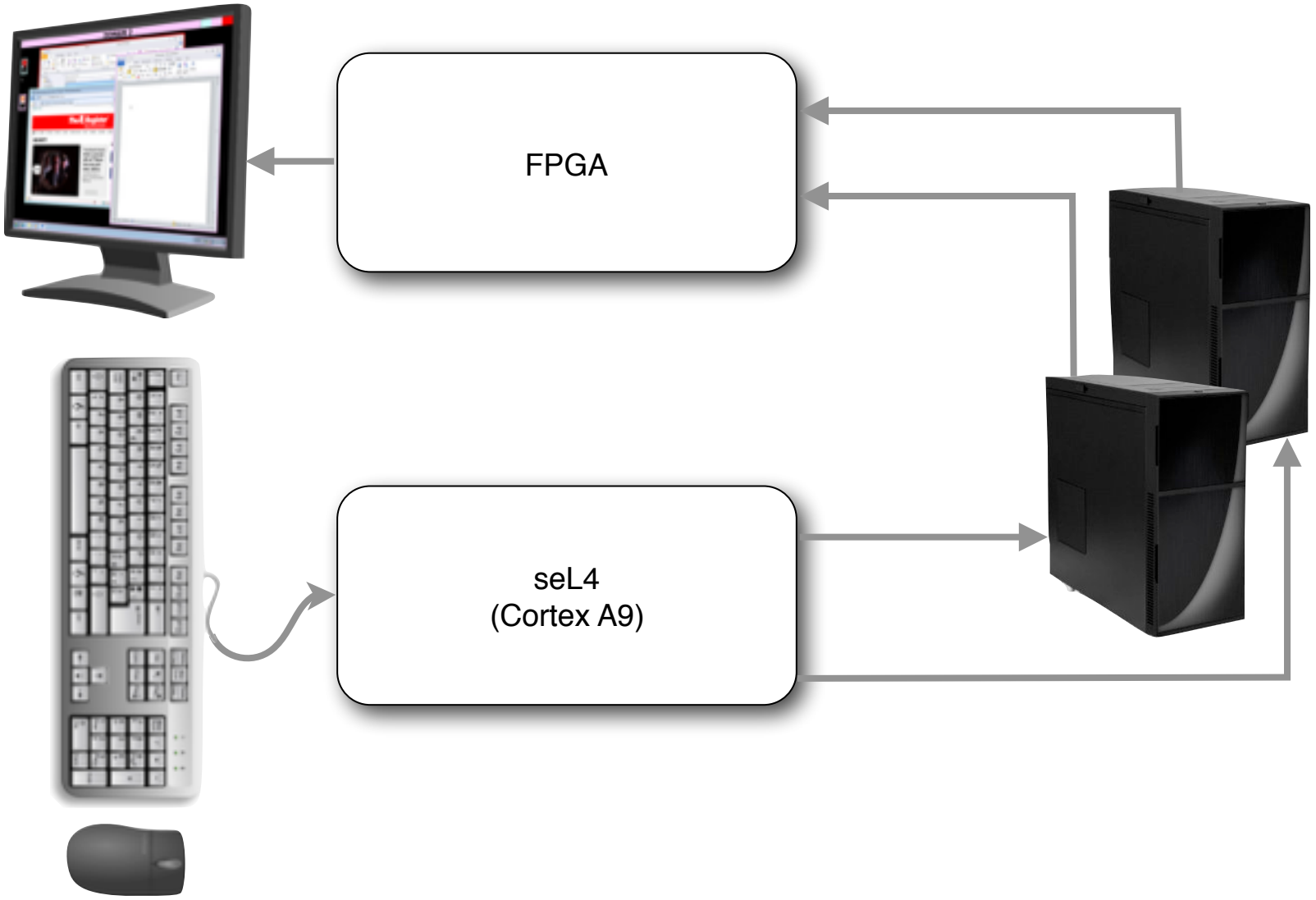

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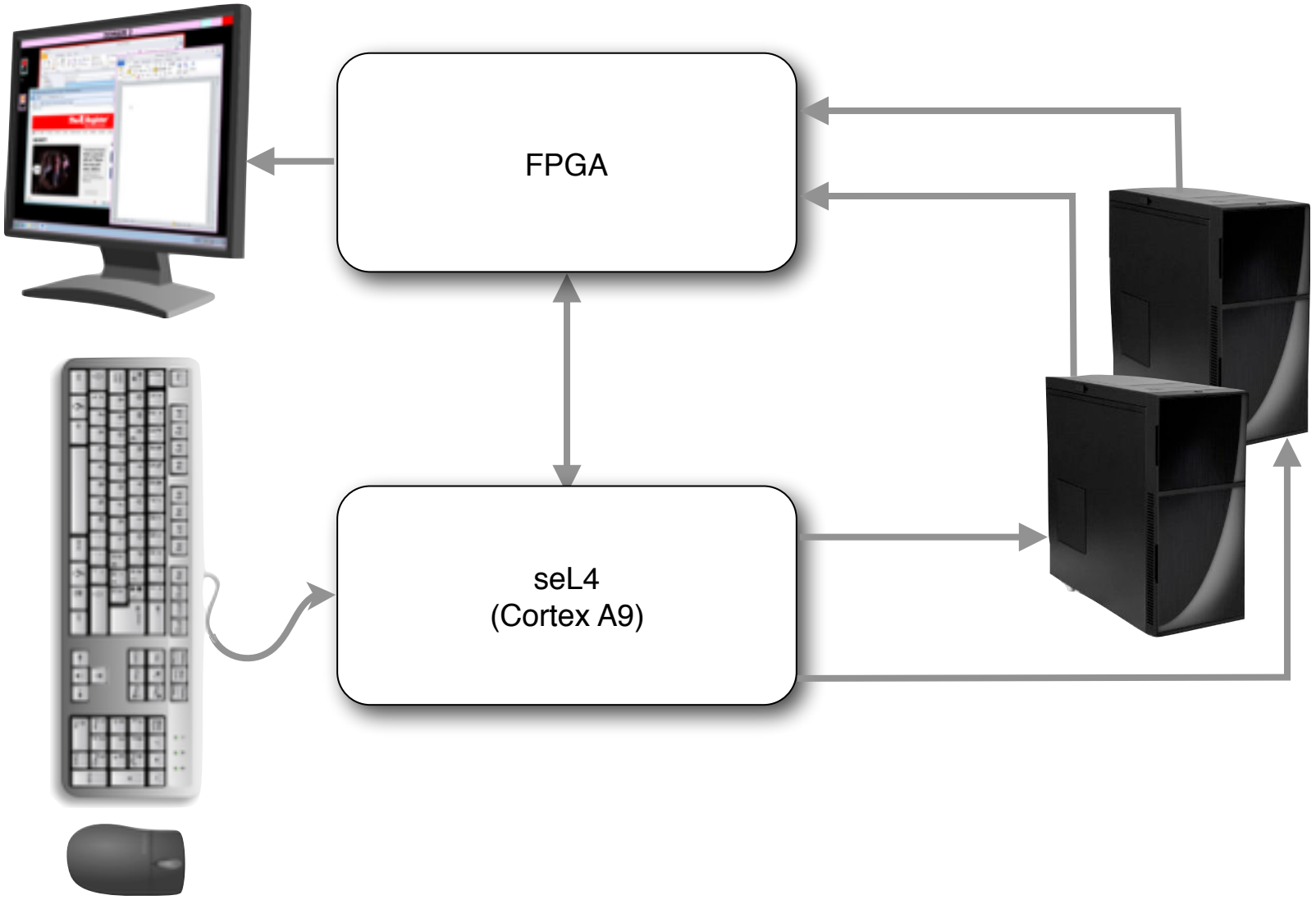

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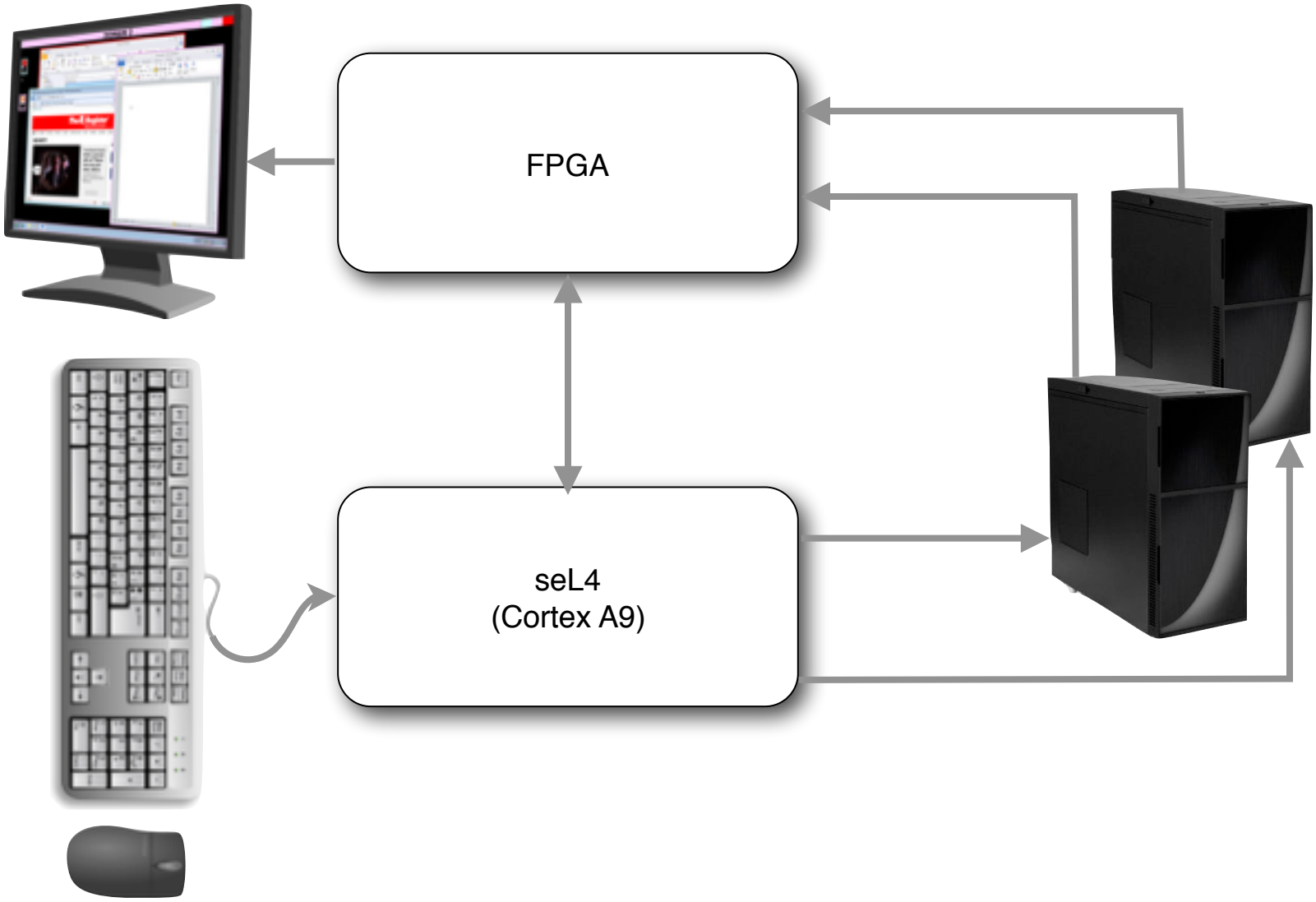

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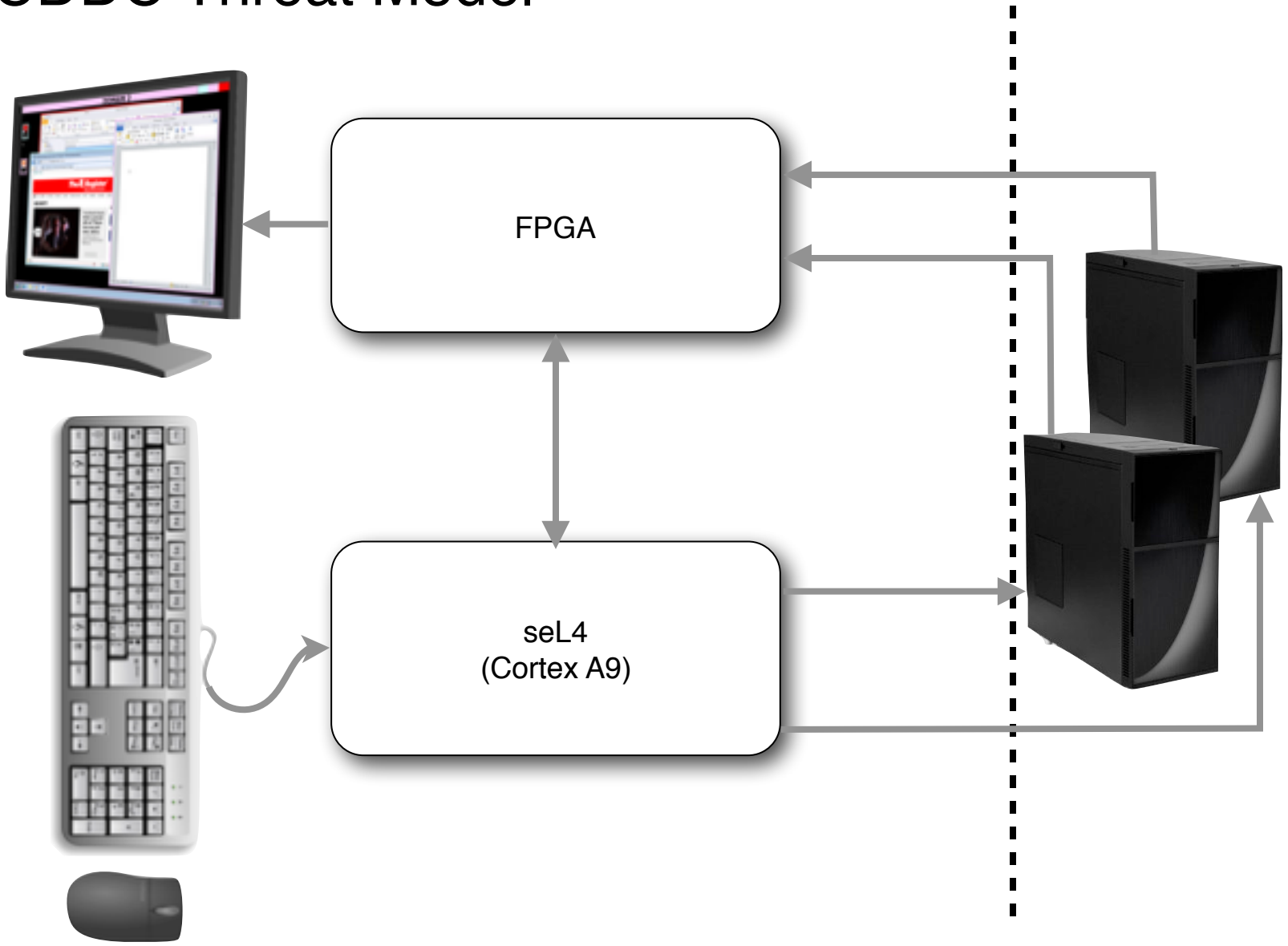

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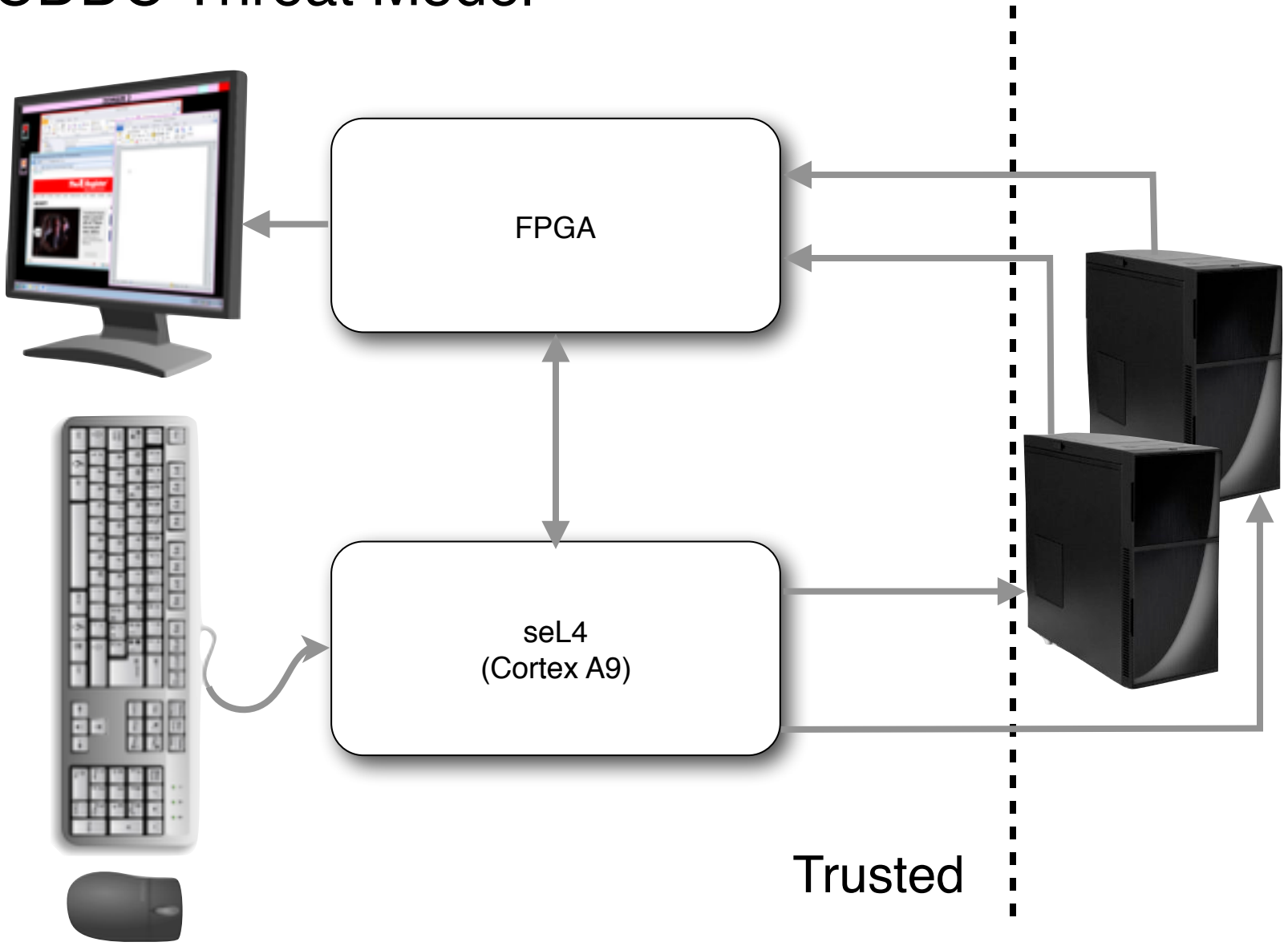

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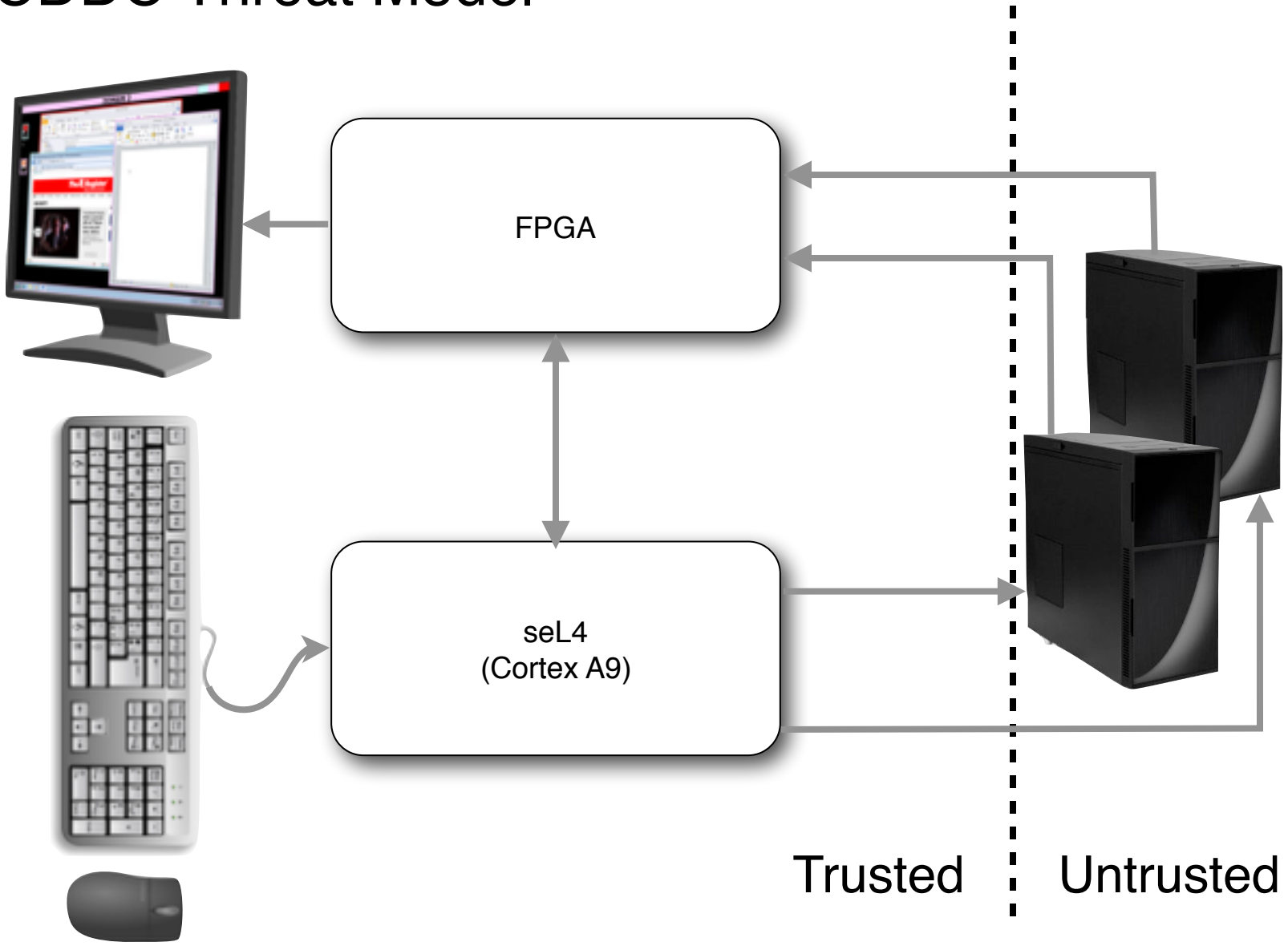

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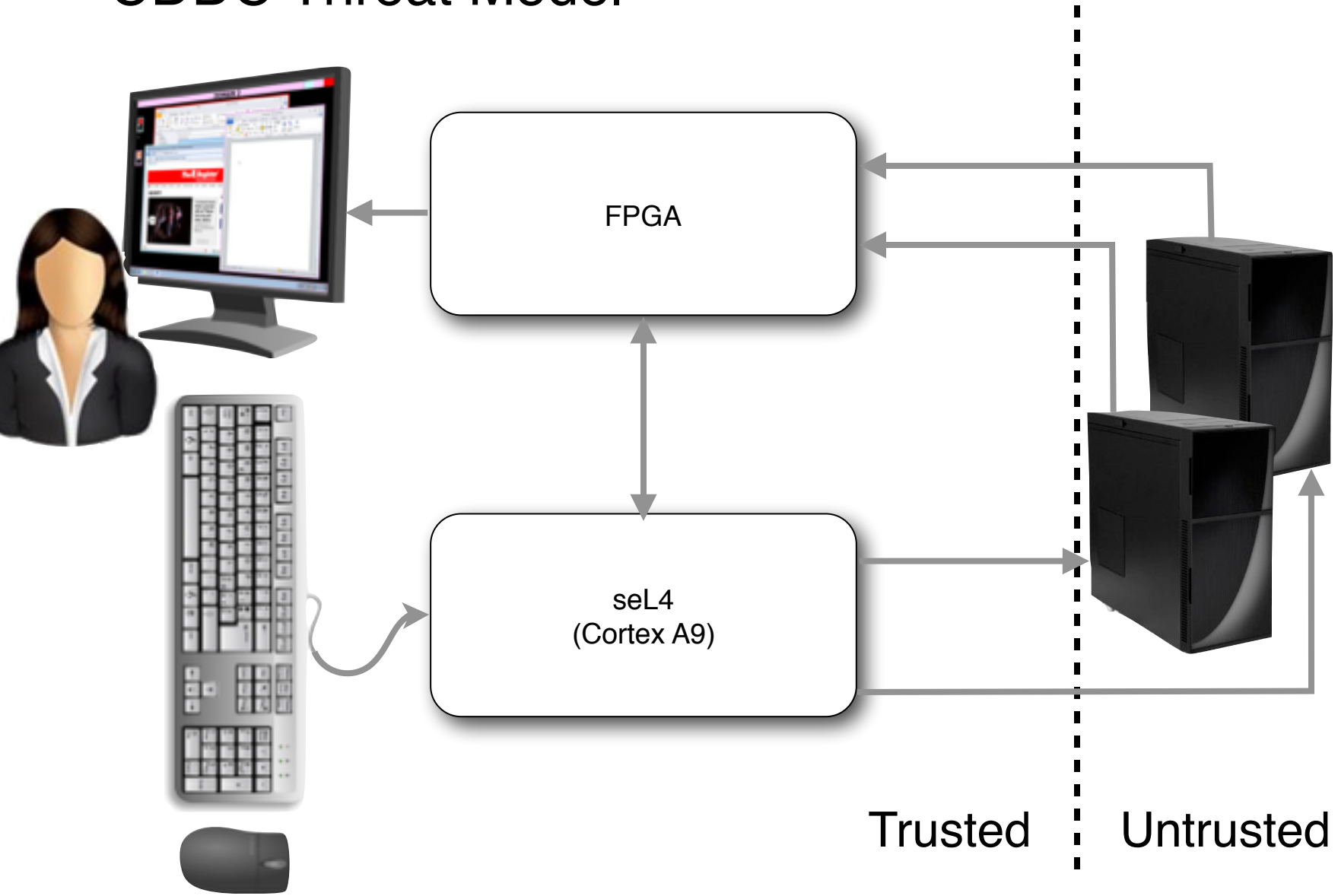
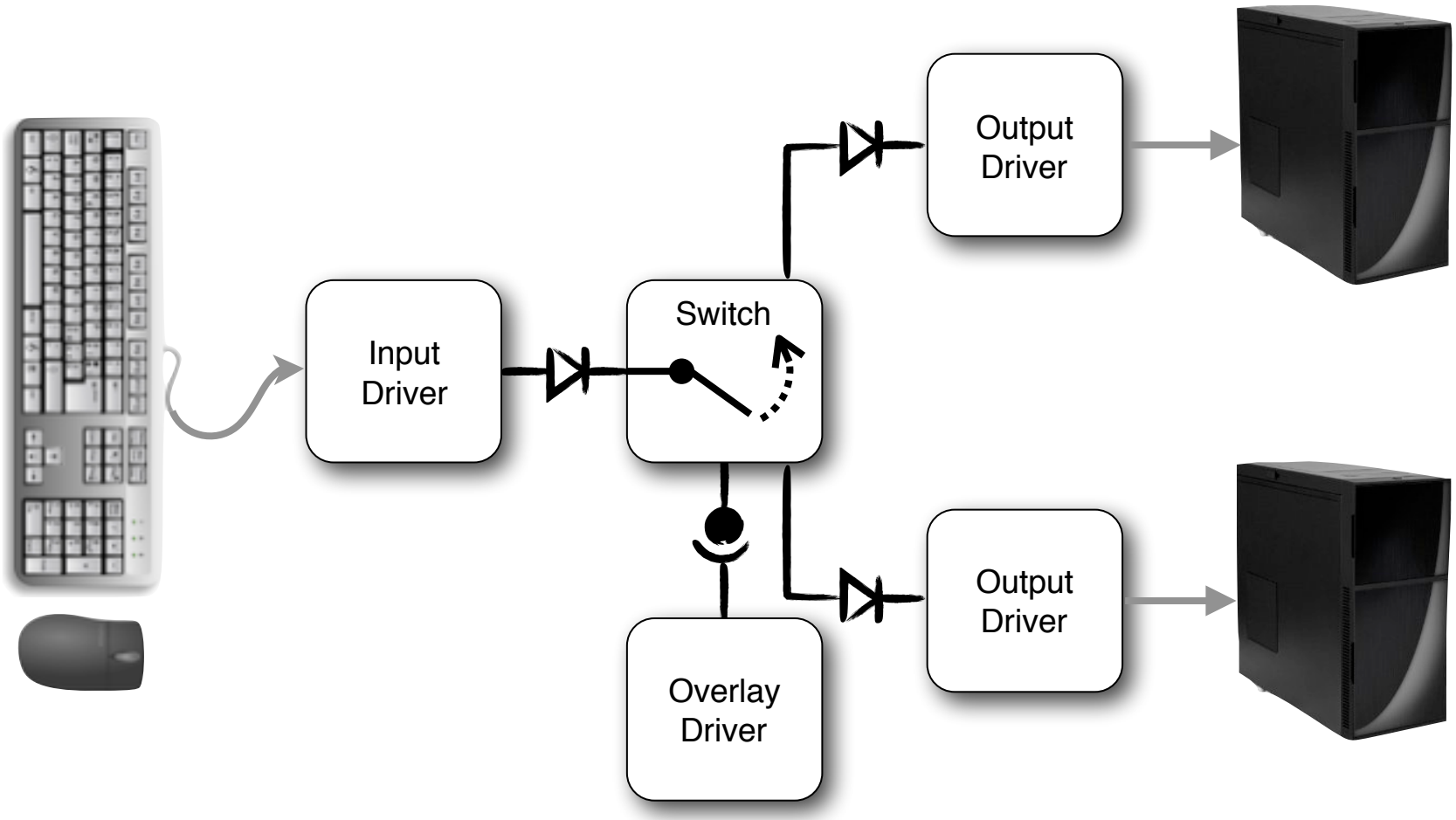
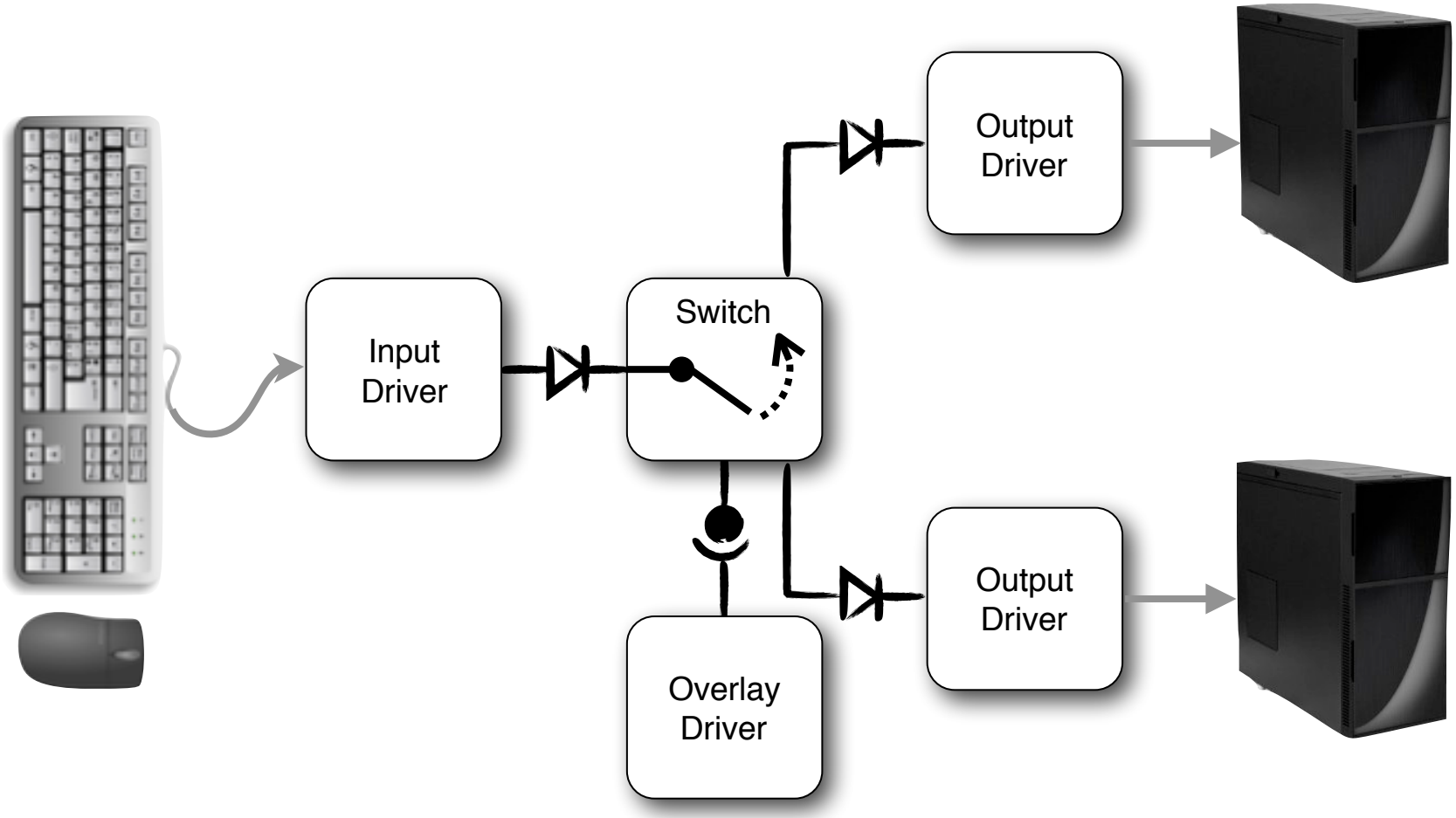


seL4-Based Software Architecture



seL4-Based Software Architecture

(ignoring device administration and configuration, plus keyboard LED control)



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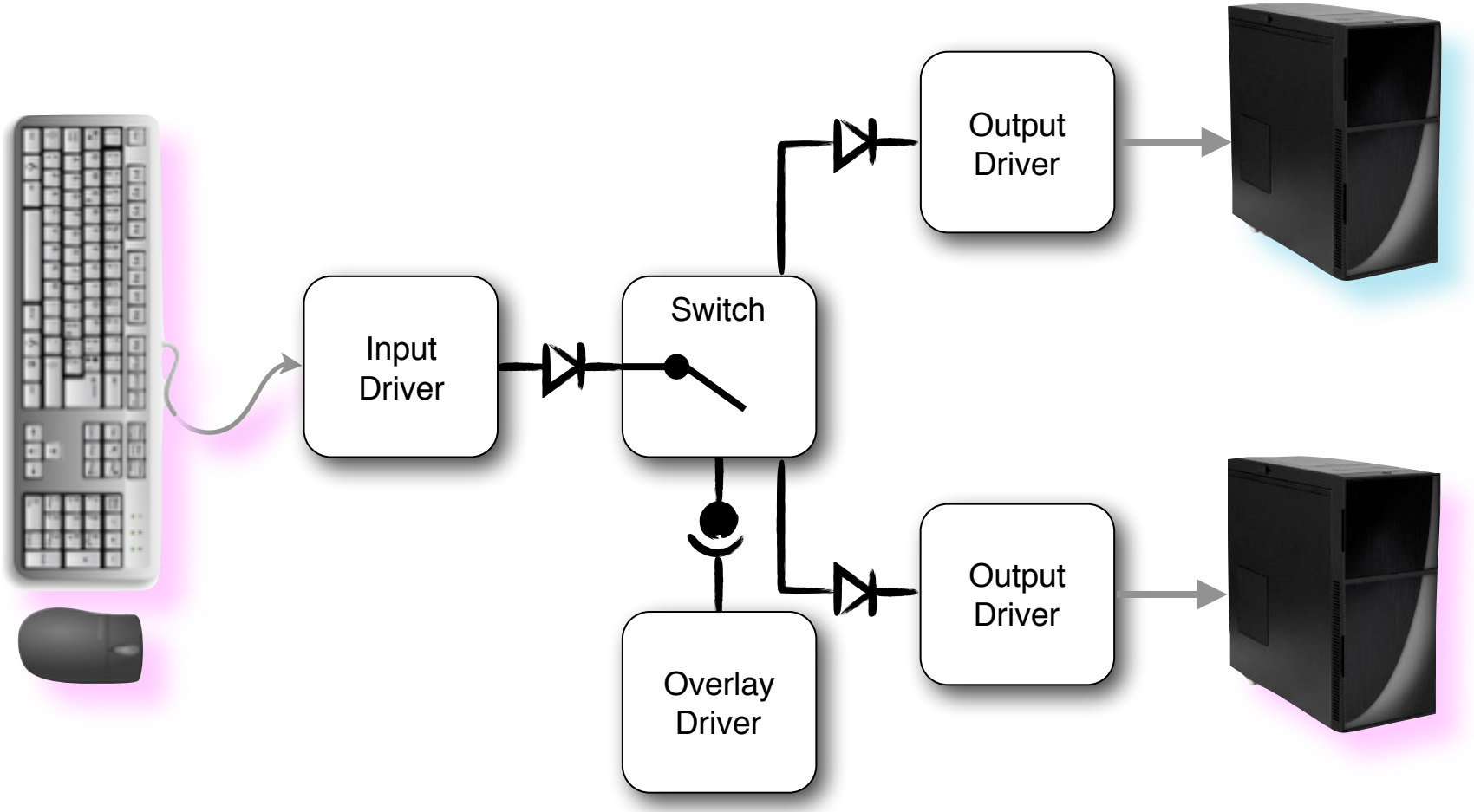

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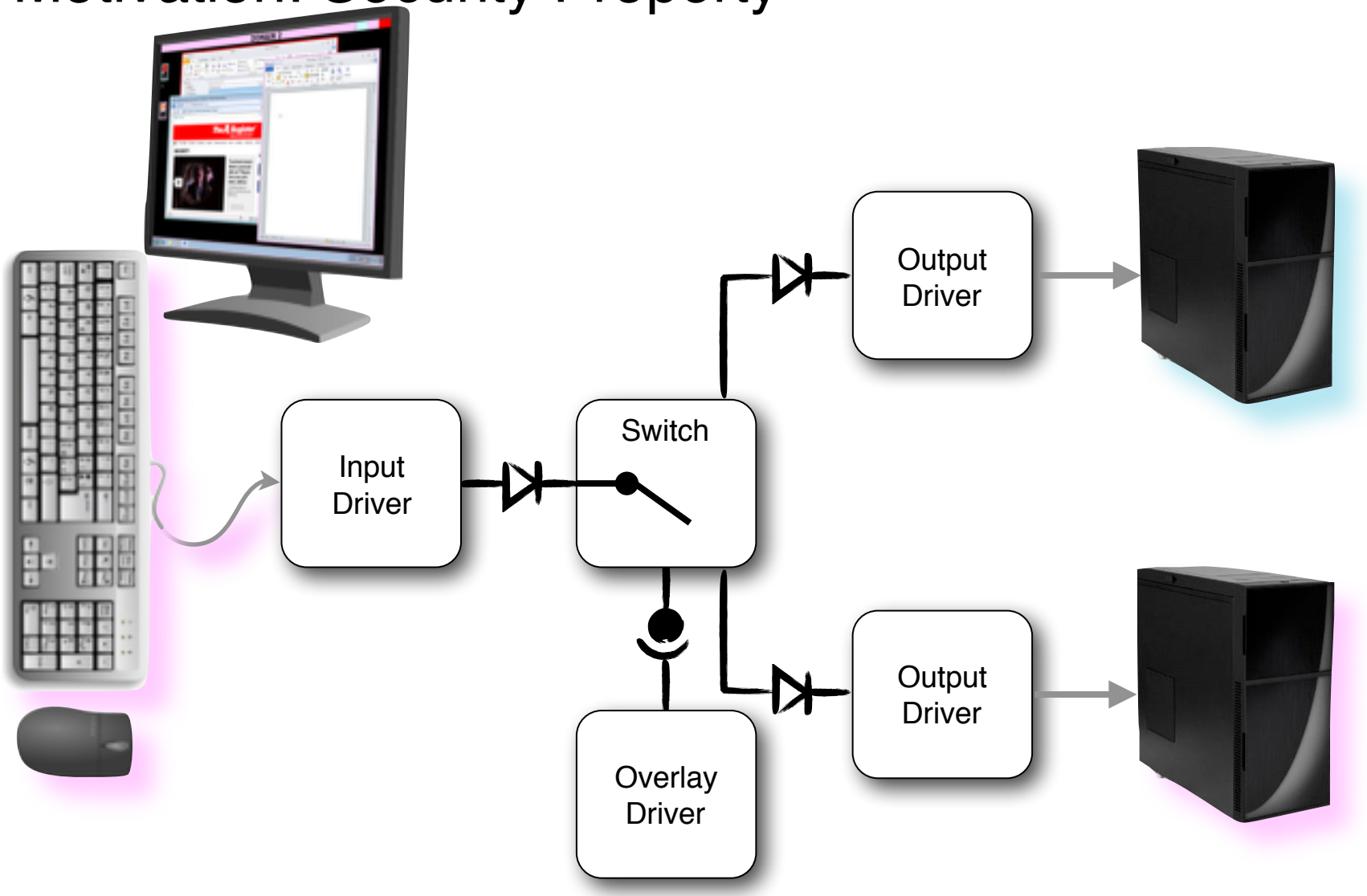

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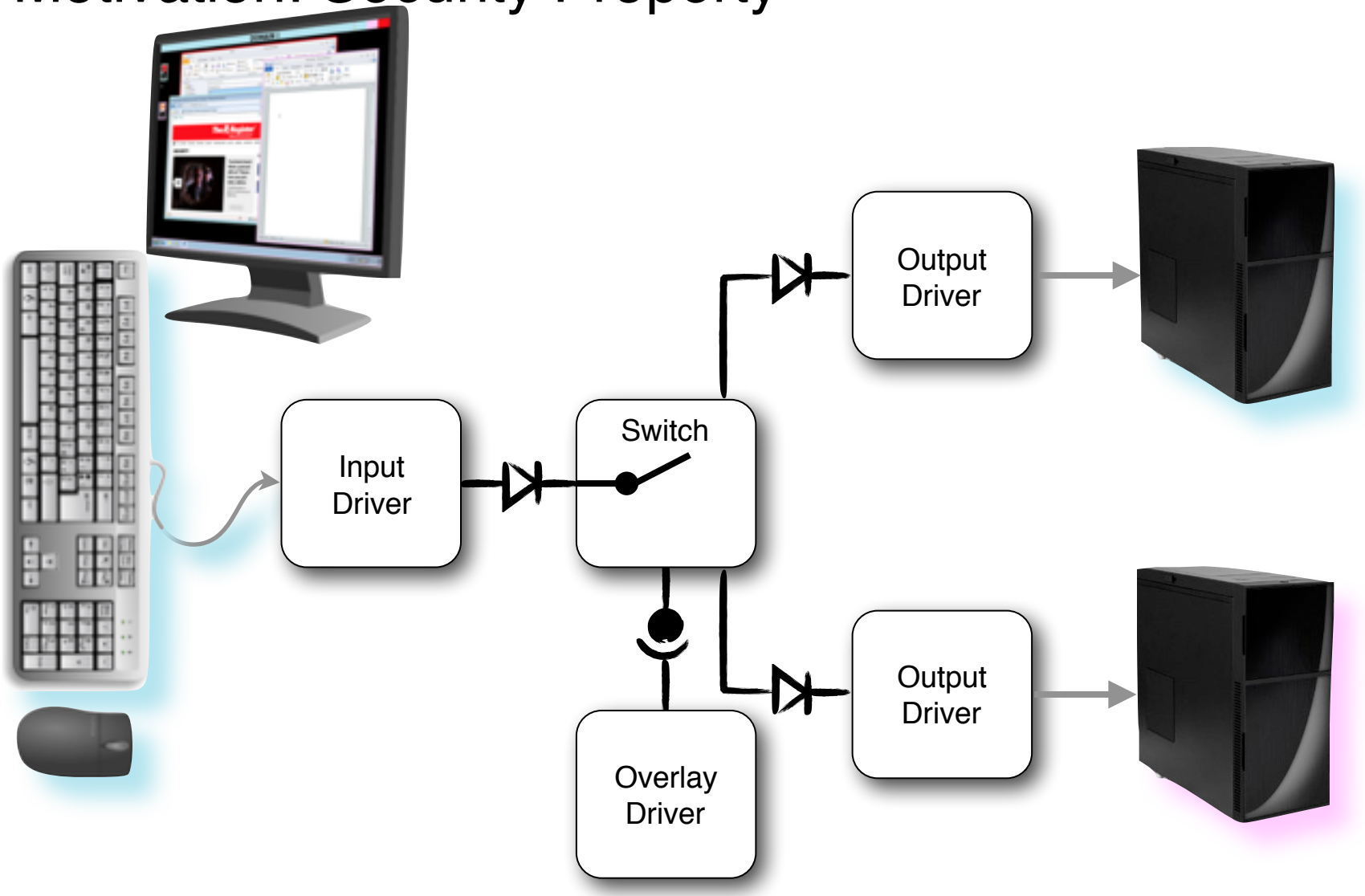

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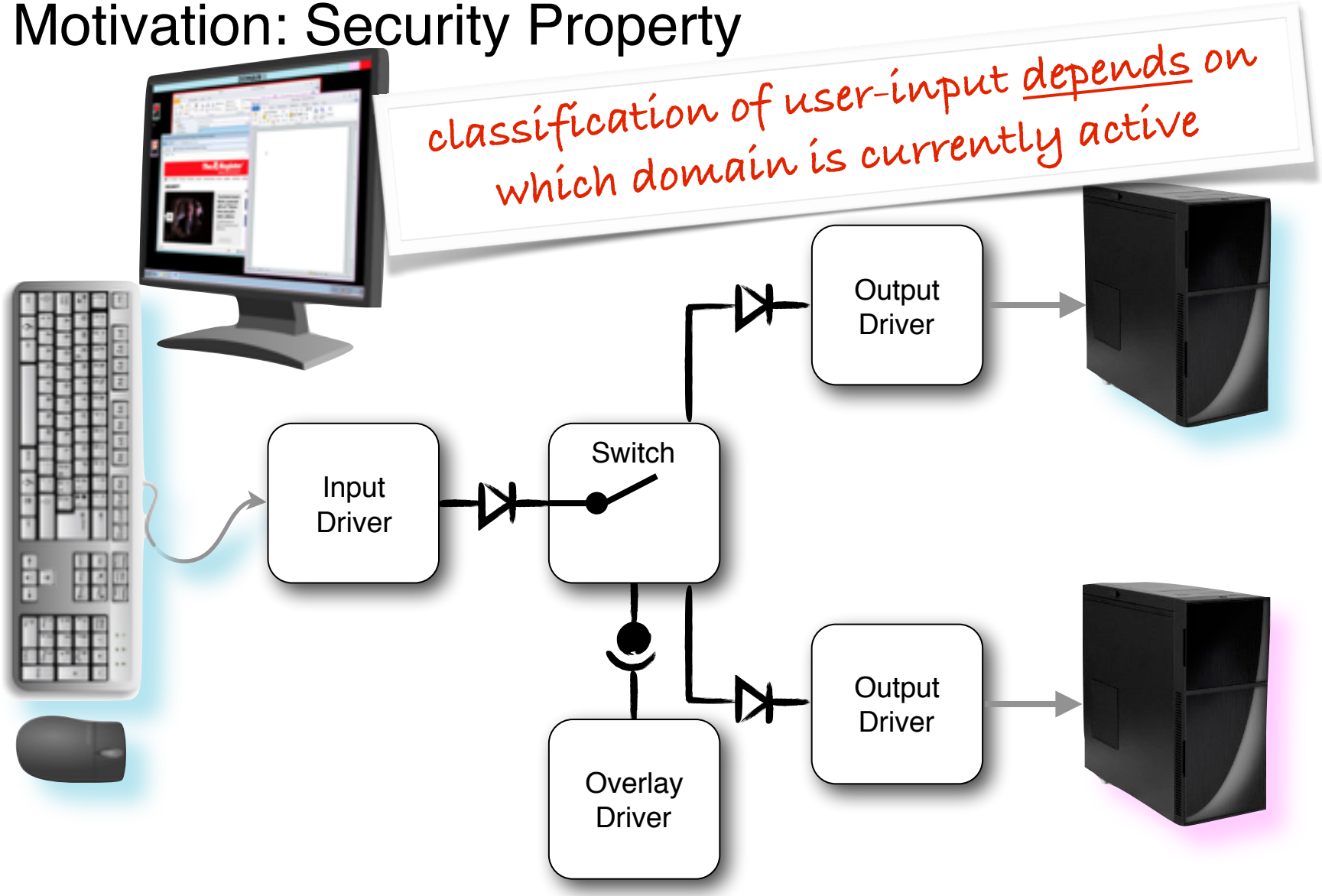

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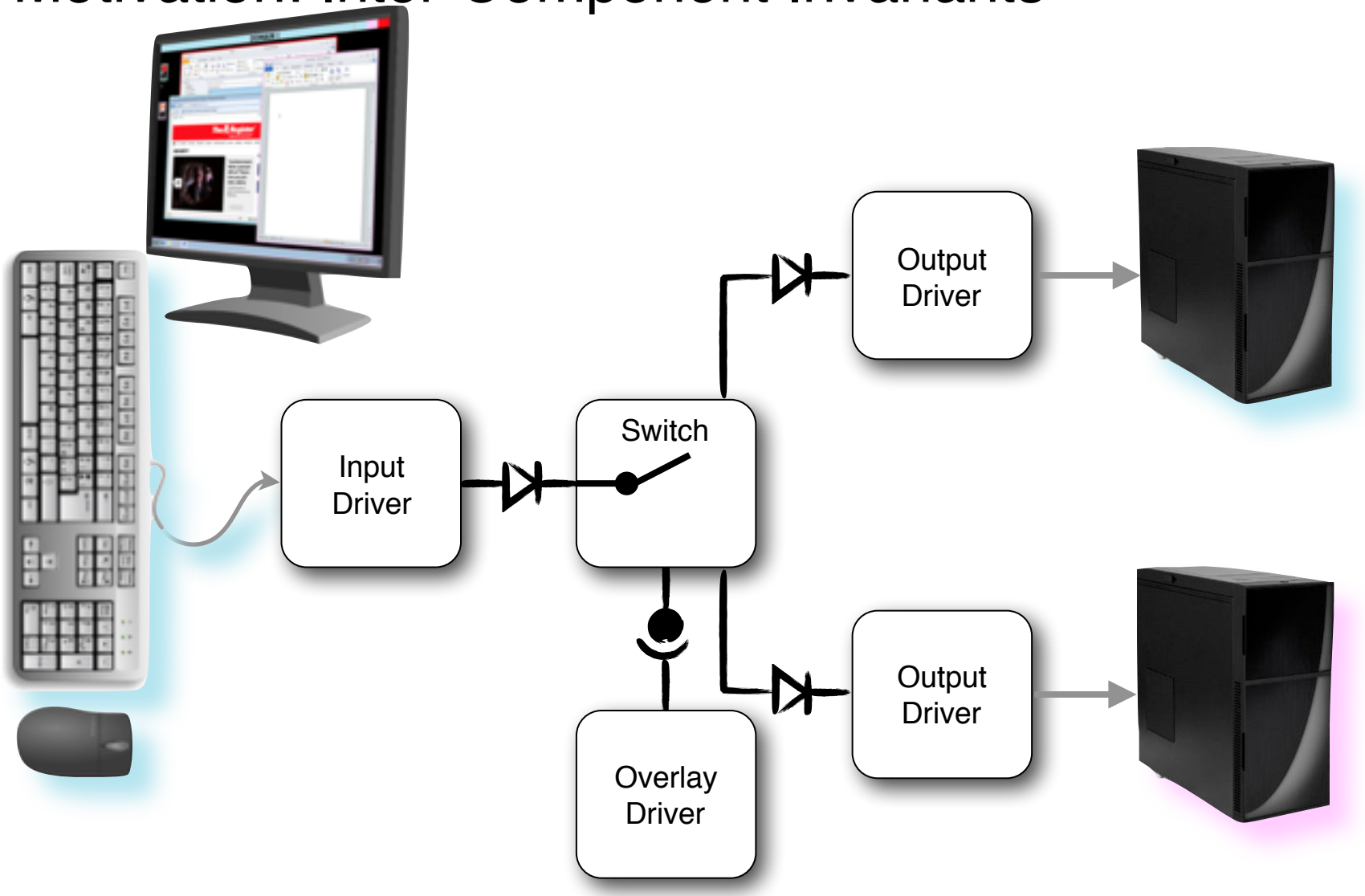

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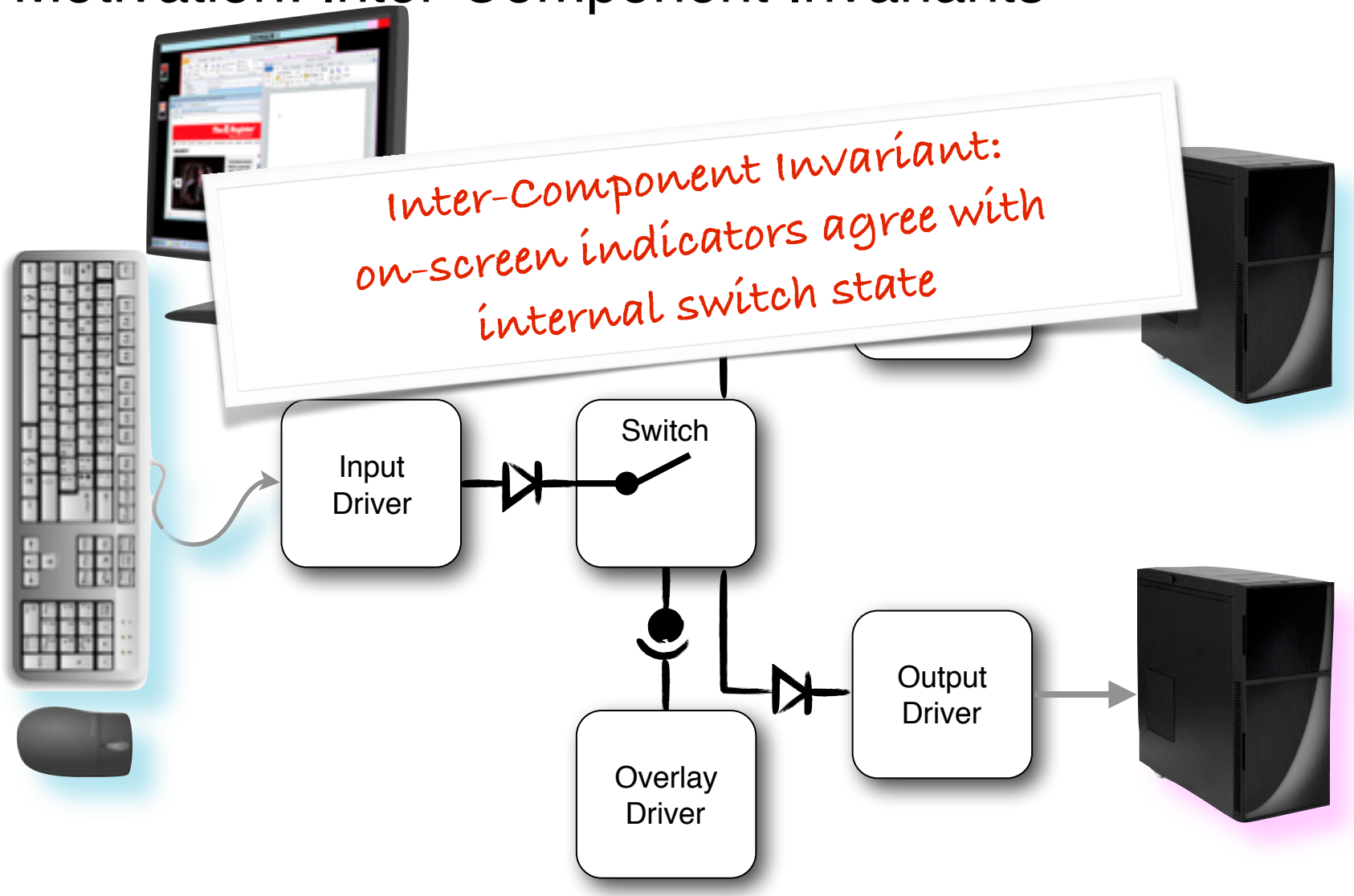

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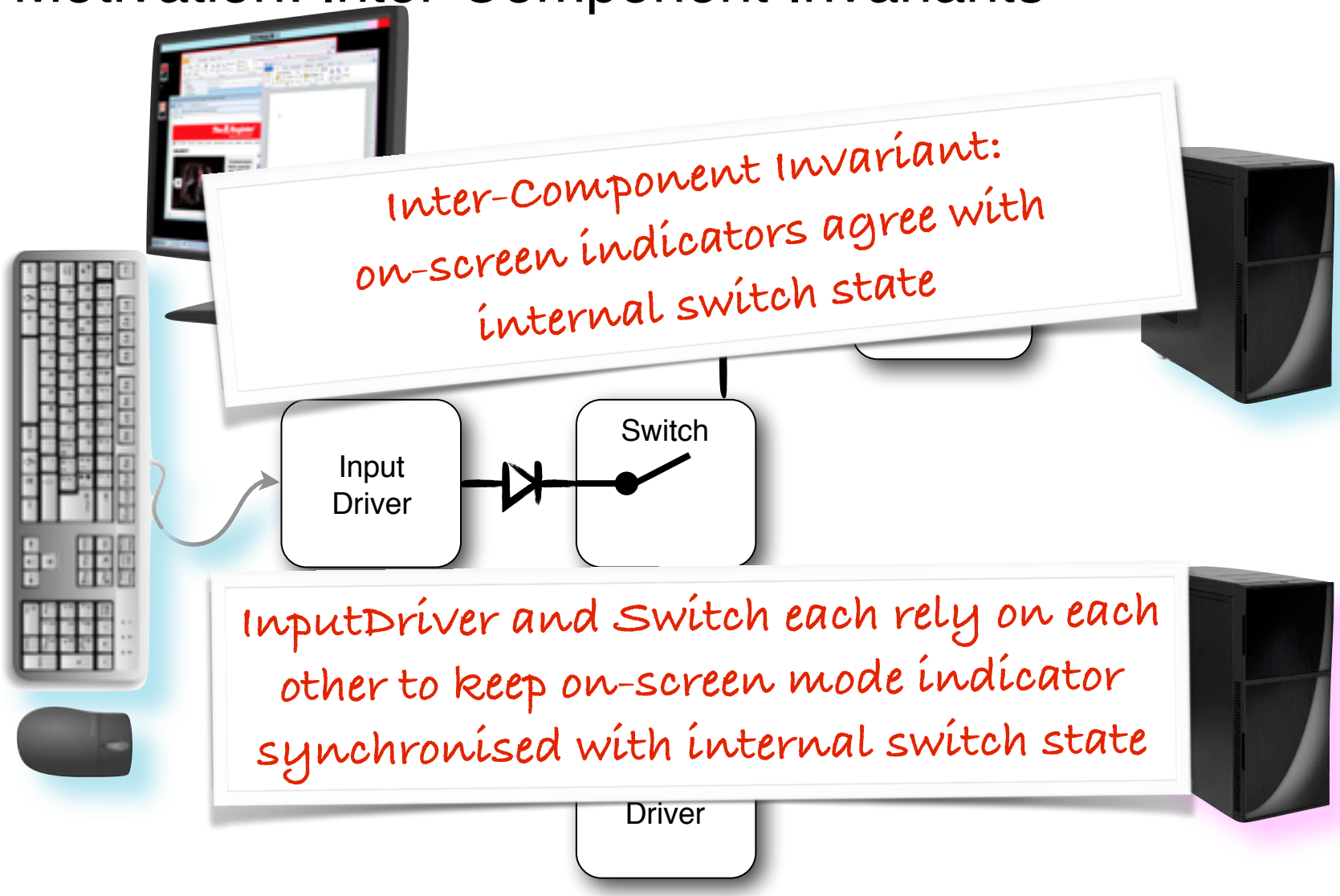

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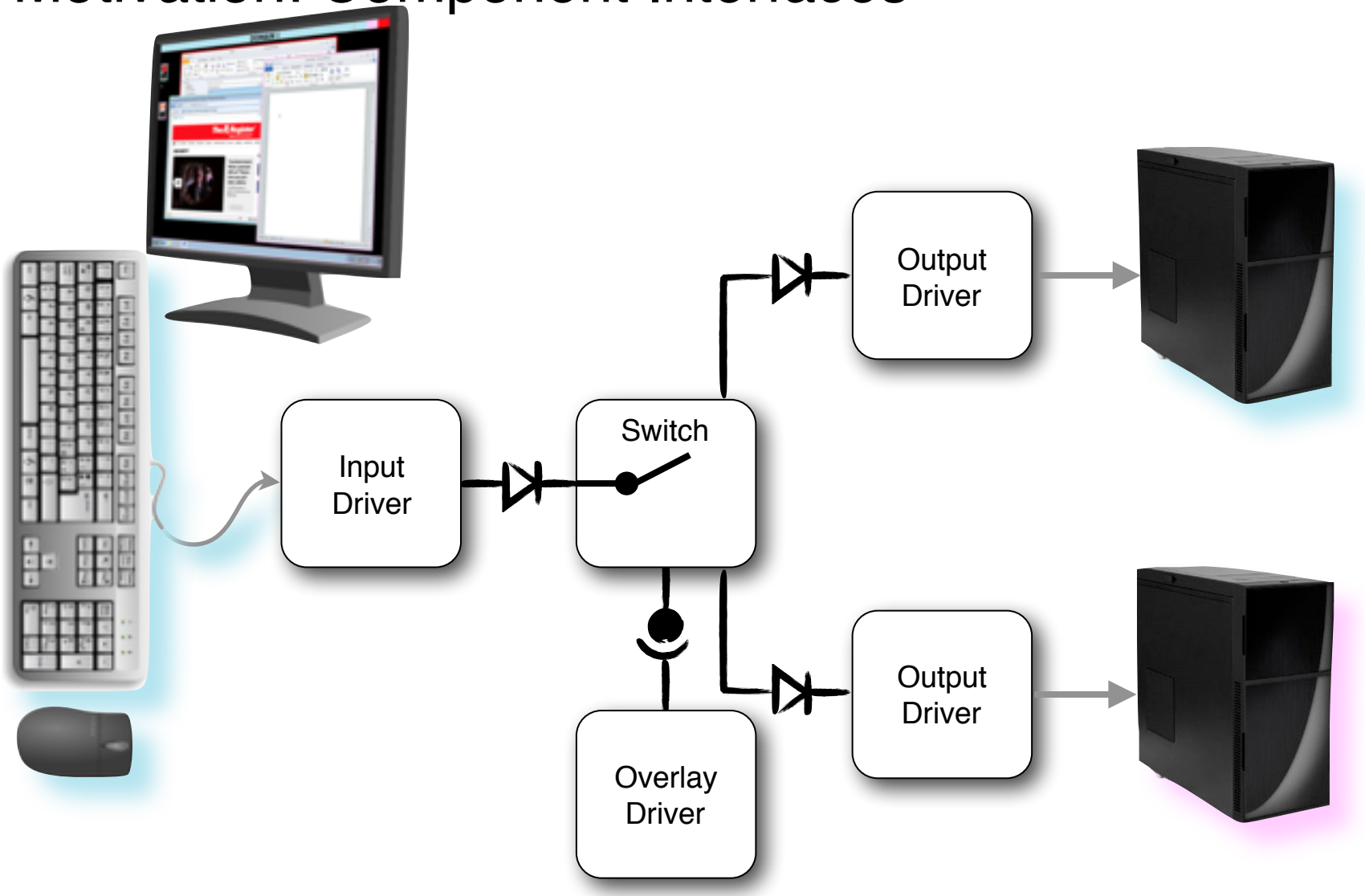

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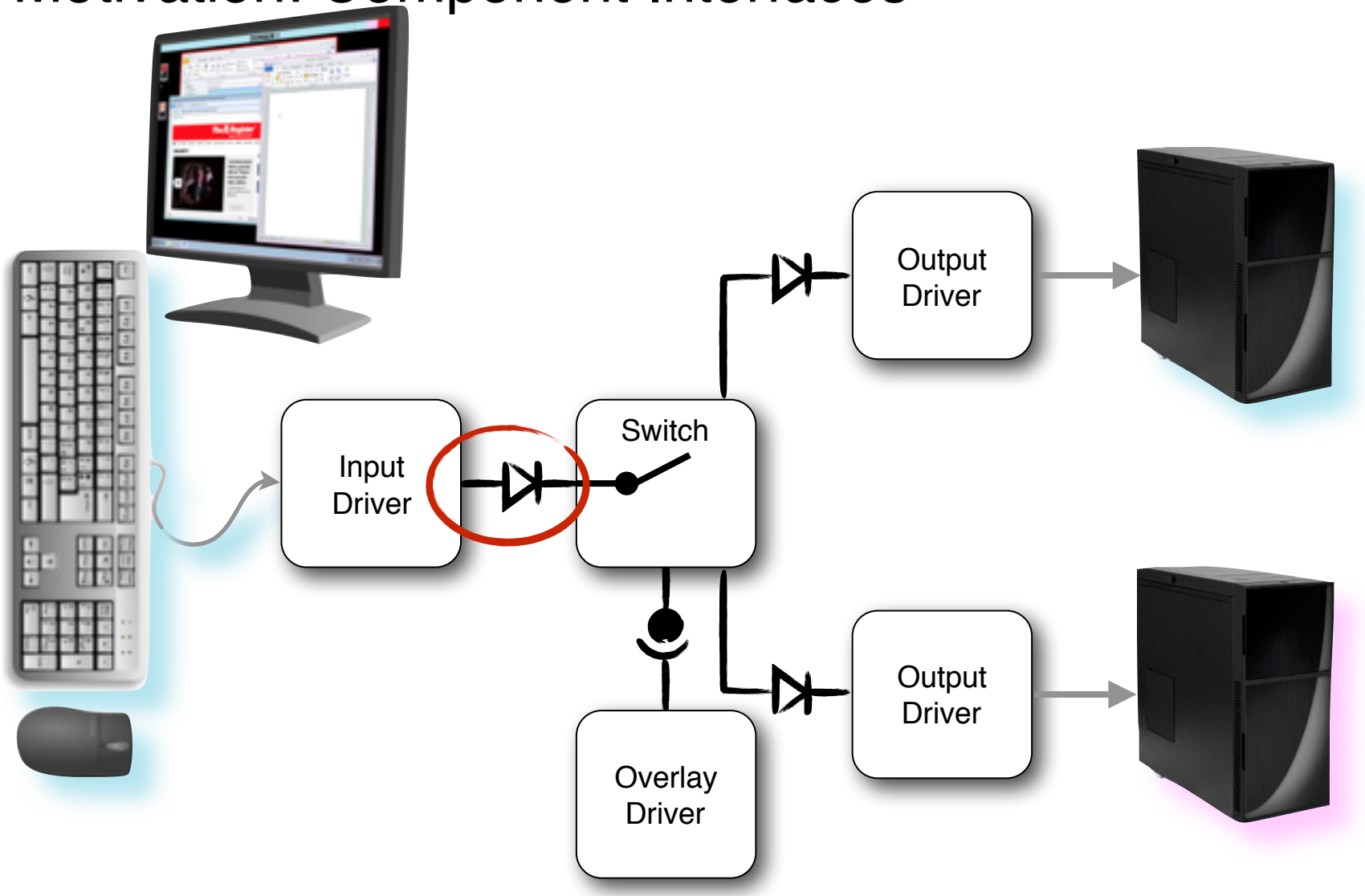

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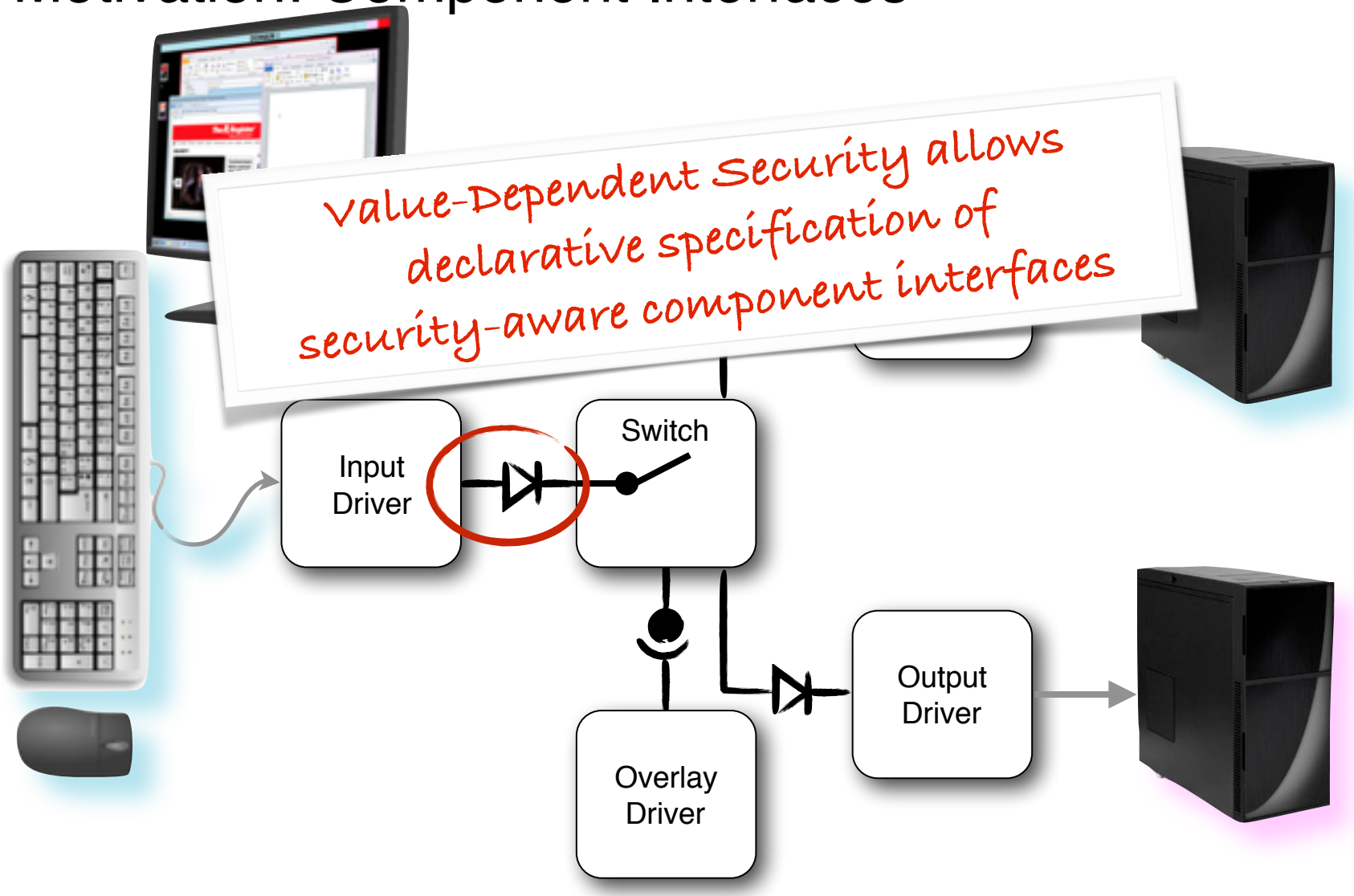

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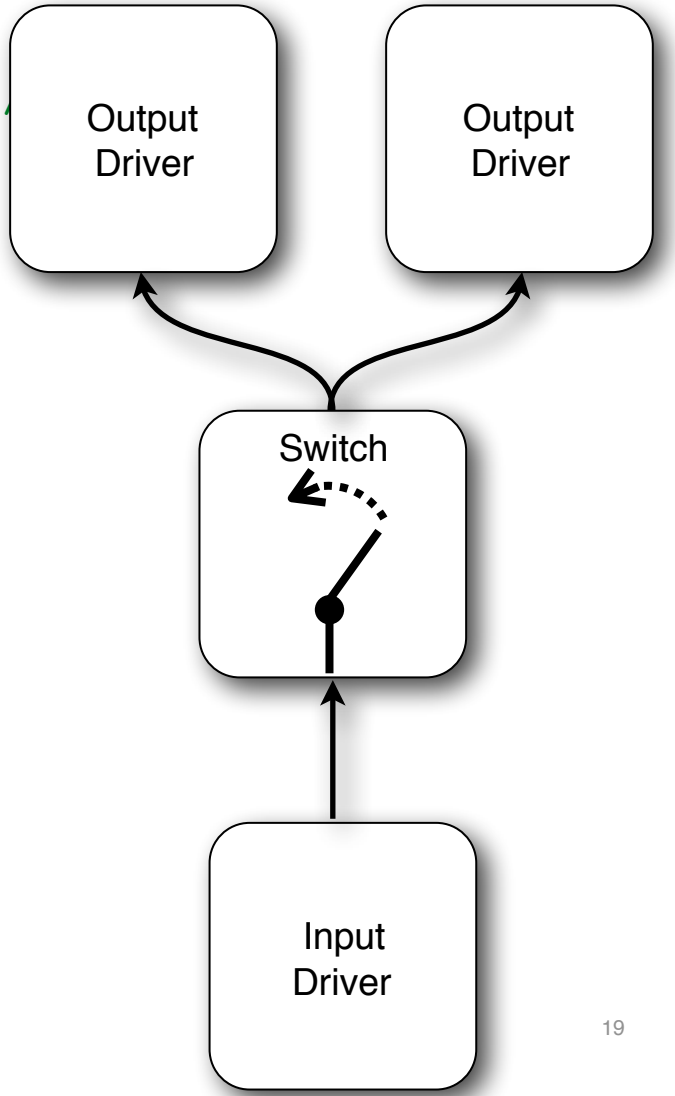

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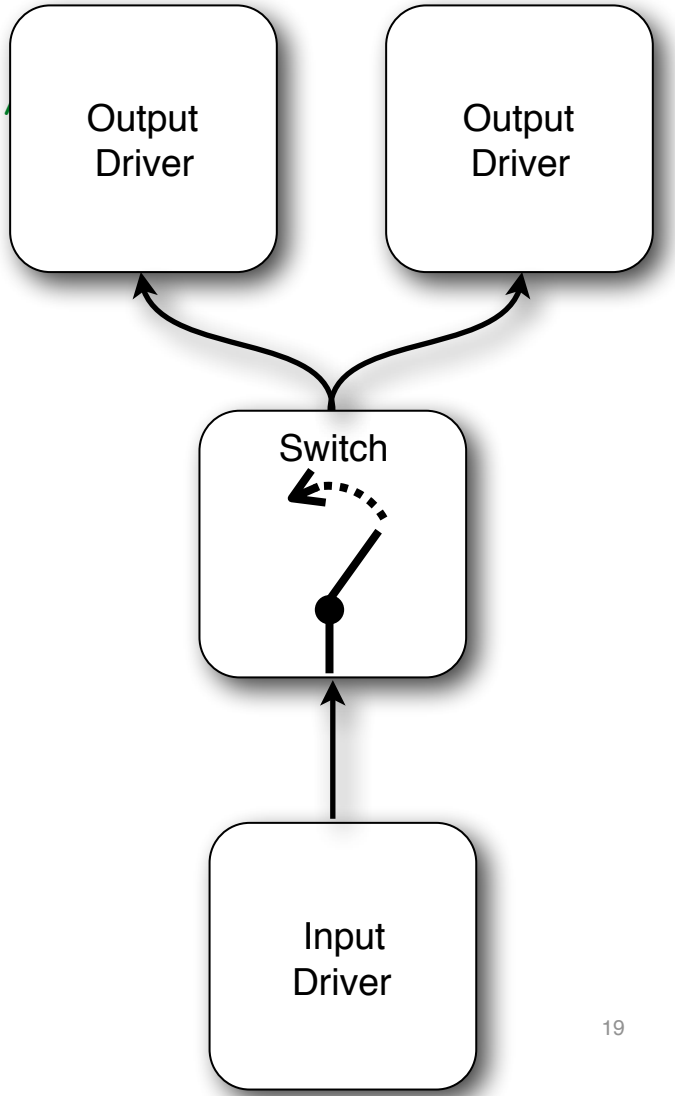

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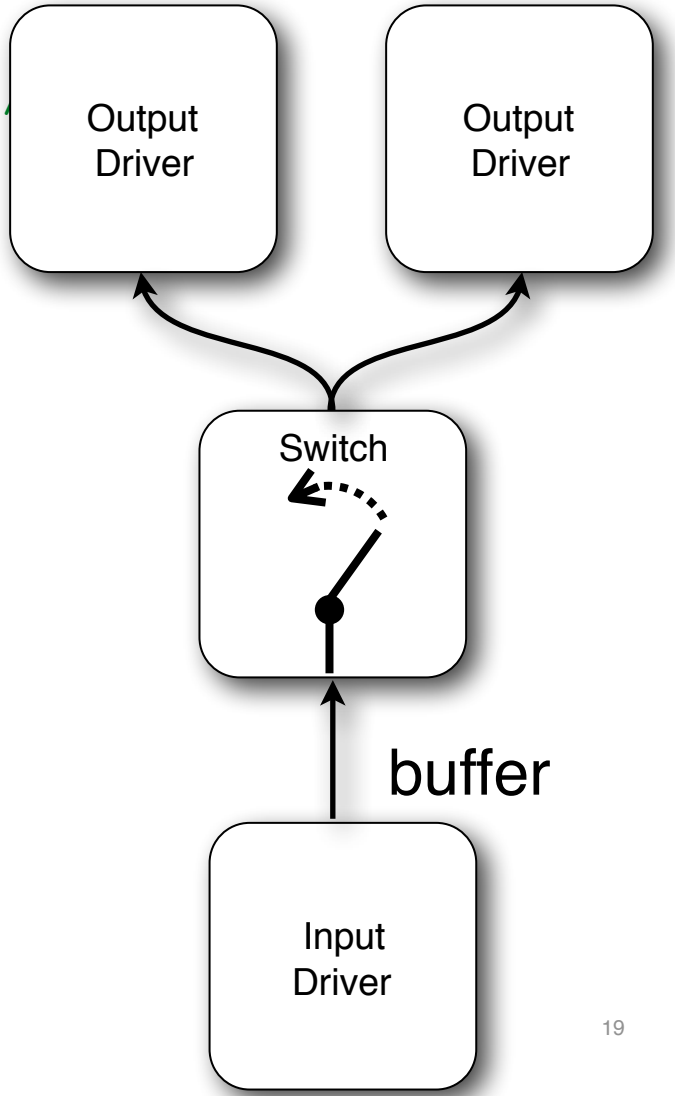

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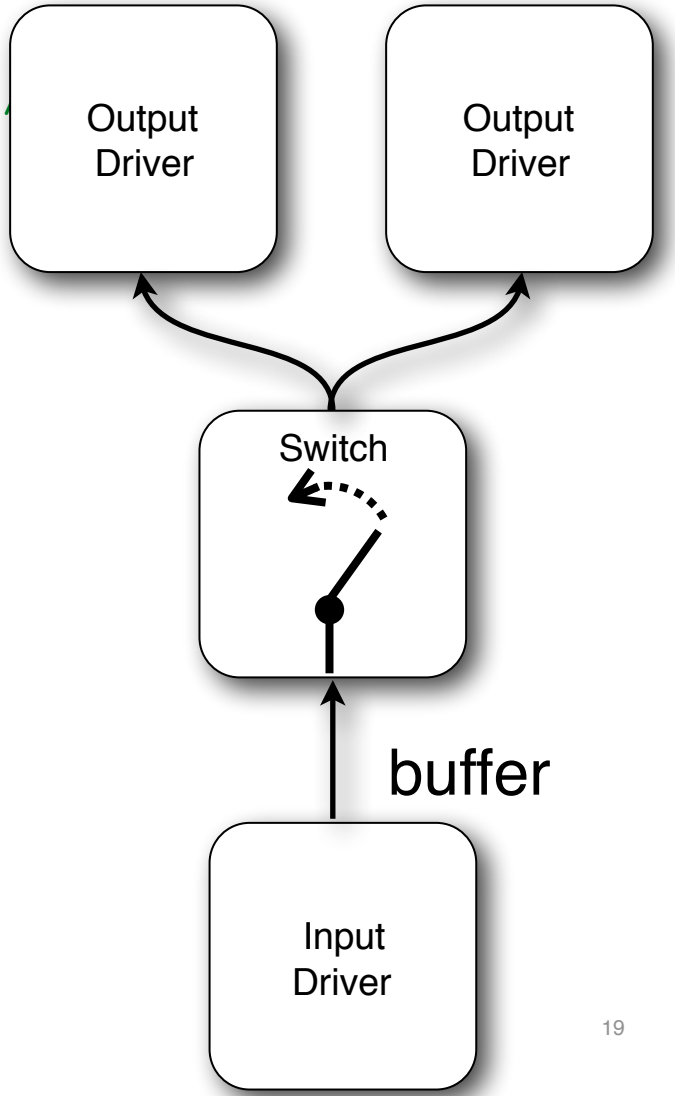

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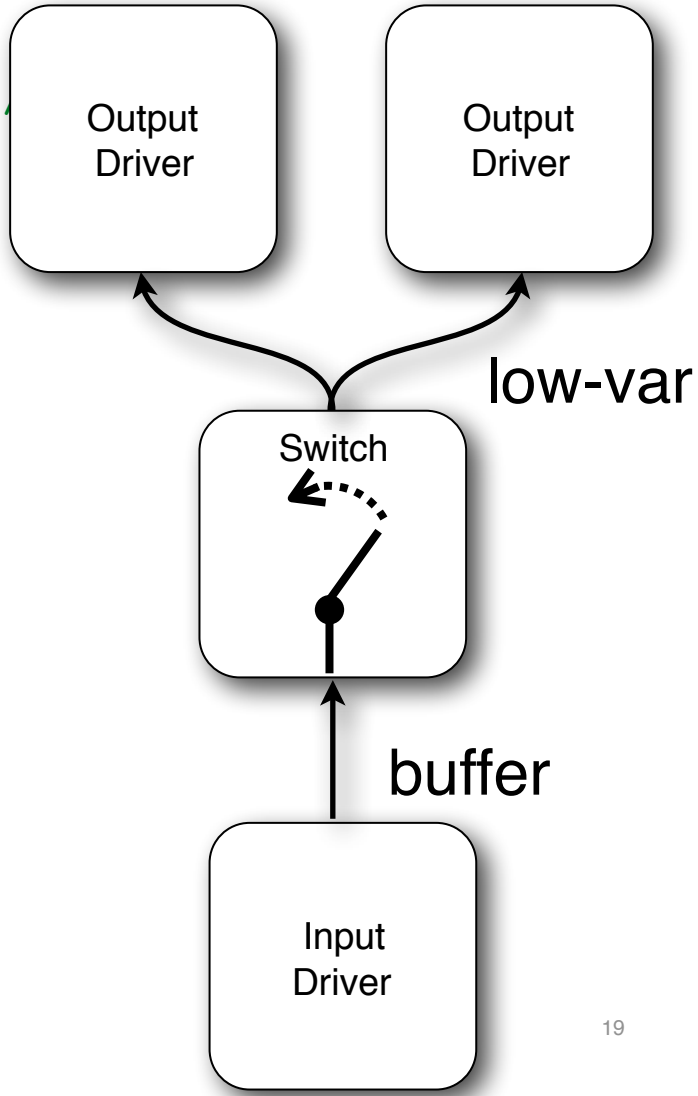

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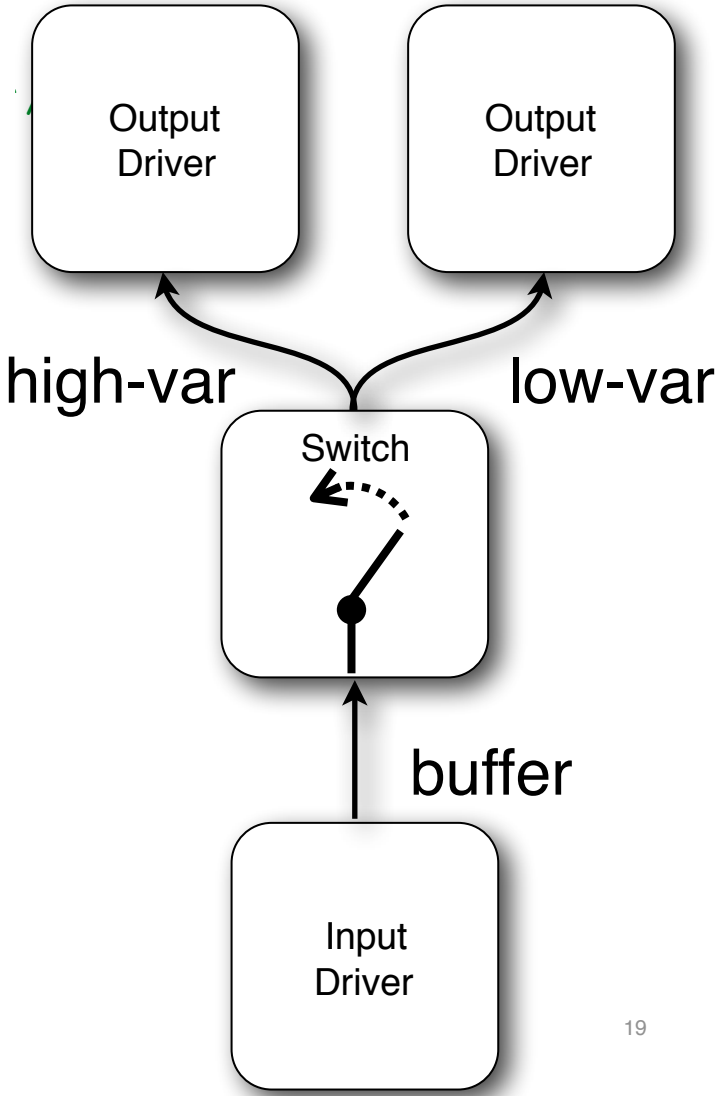

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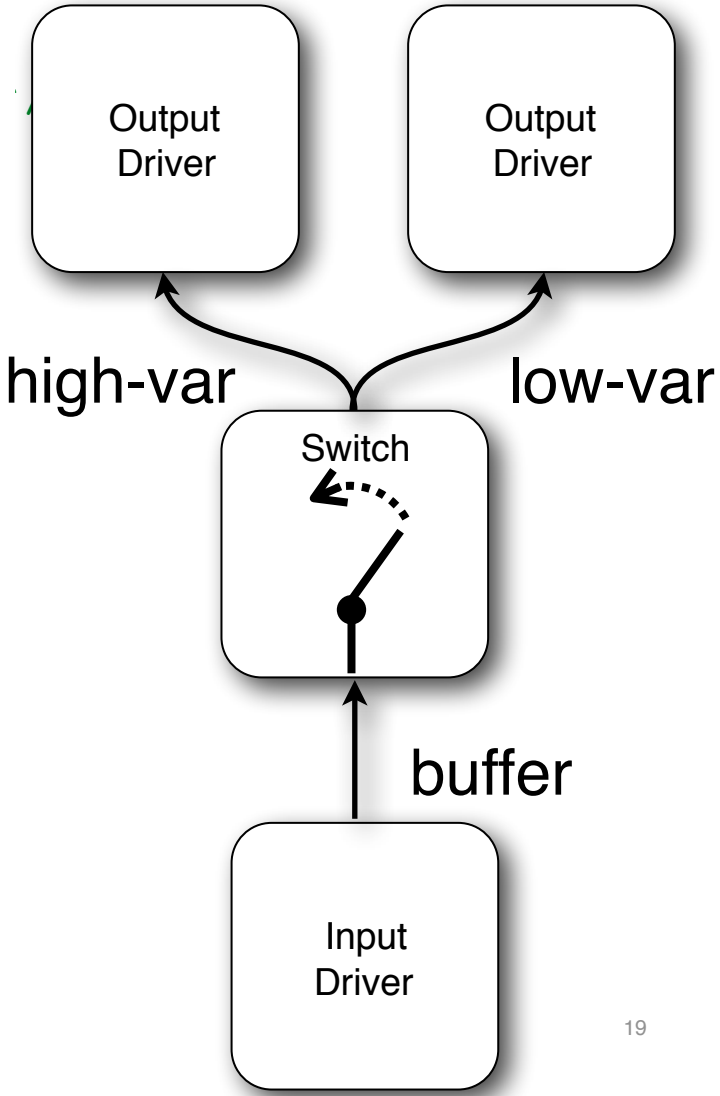

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what if somebody else modifies **sMode** here?

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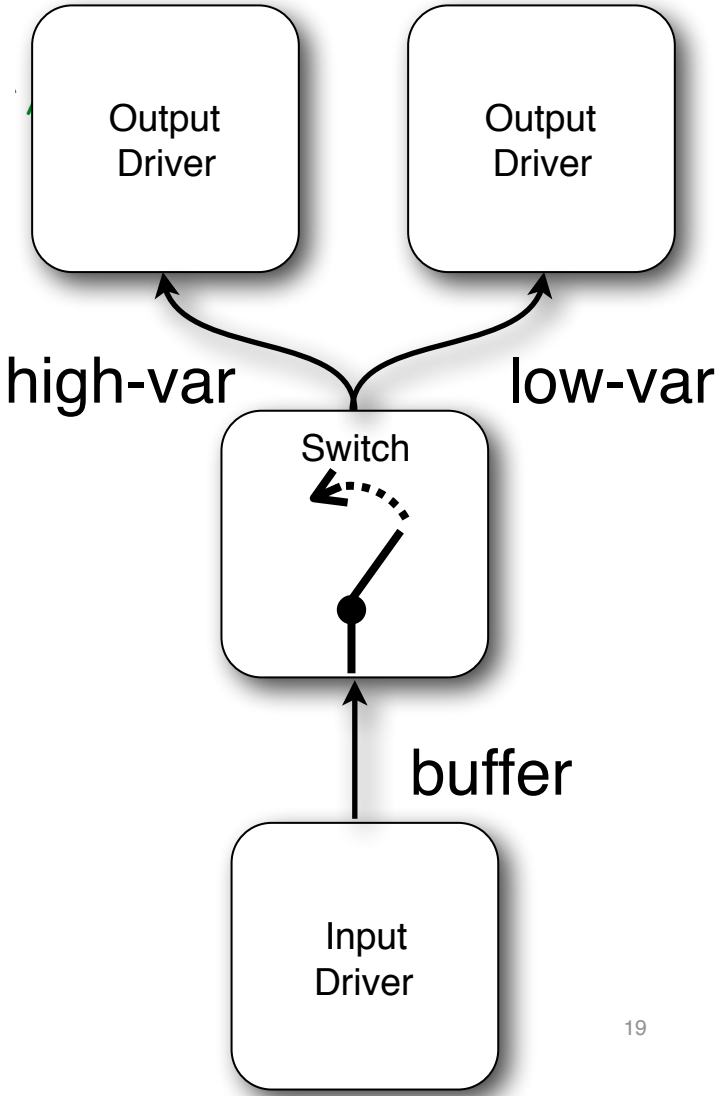

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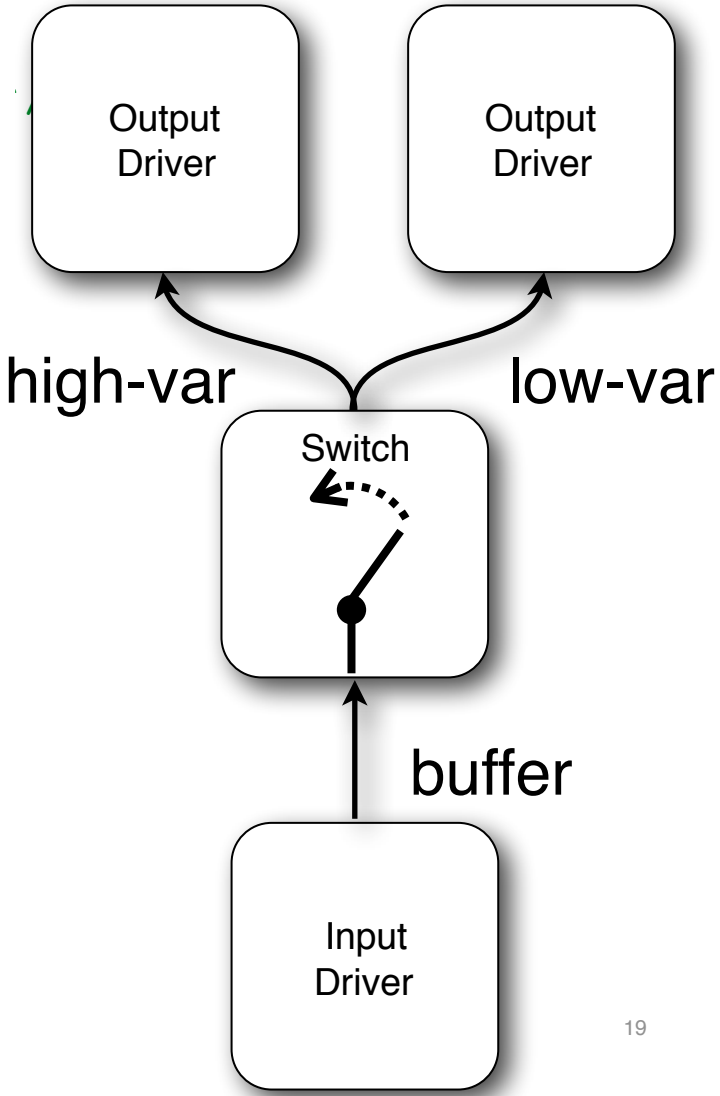

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what if **temp** holds High data here and somebody else reads it?

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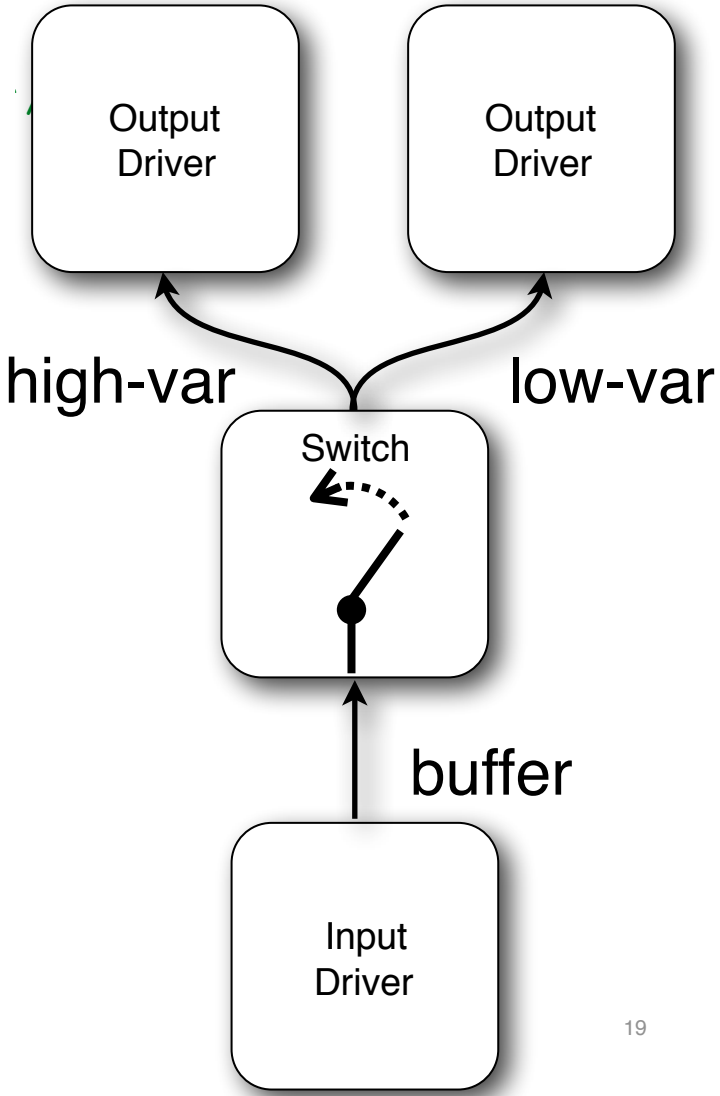

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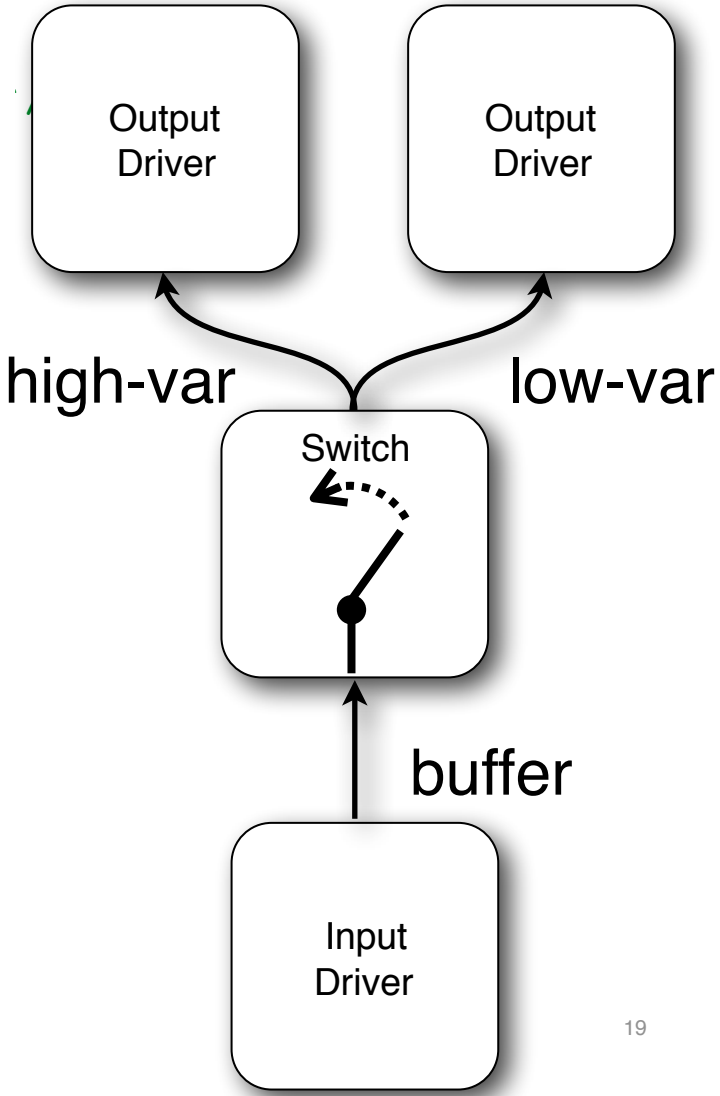
  high-var := temp
endif;
temp := 0
```

sMode *is switch's mode*

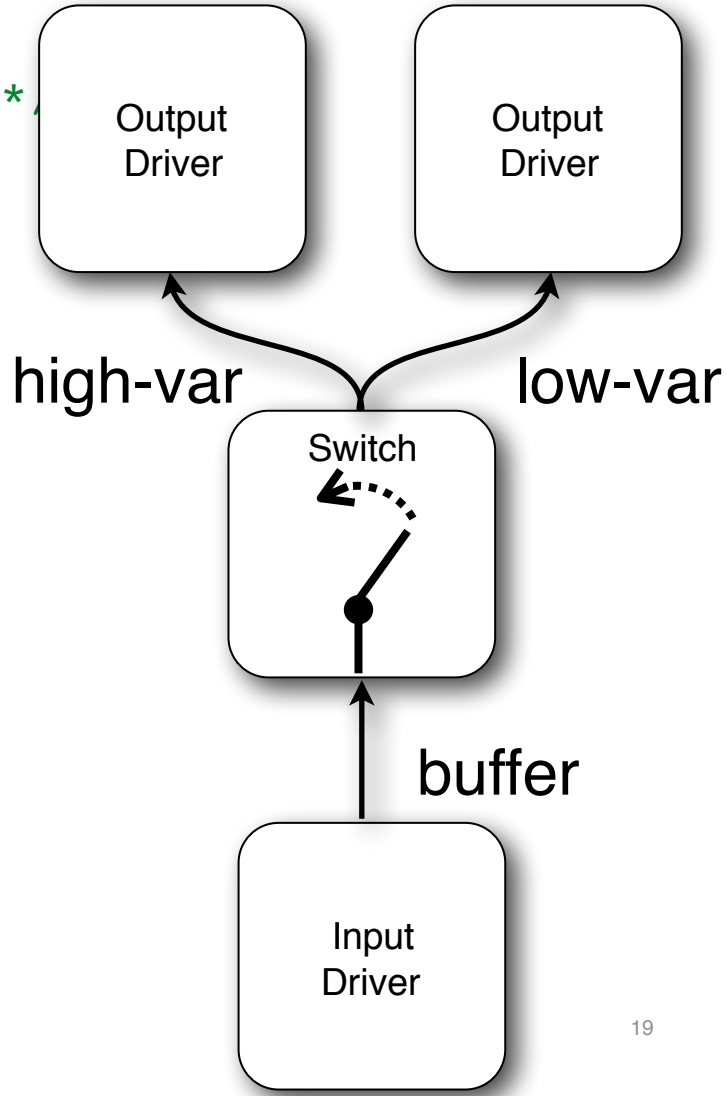


Motivation: Shared Memory Concurrency

Switch (idealised, obviously):

```
/* {dMode,sMode,temp} += AsmNoRW */
/* acquire (dMode == sMode) */
temp := buffer;
if sMode == 0 then
  low-var := temp
else
  high-var := temp
endif;
temp := 0
```

sMode *is switch's mode*



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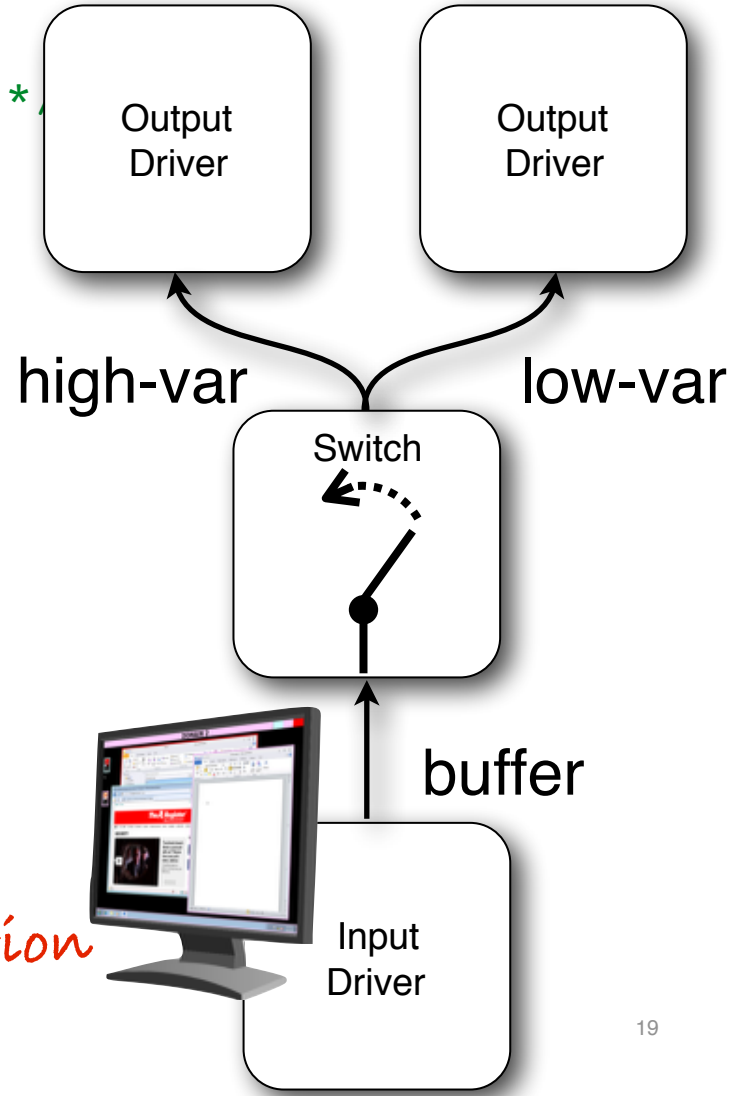

sMode *is switch's mode*

dMode *defines* buffer*'s classification*

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else
  high-var := temp
endif;
temp := 0
```
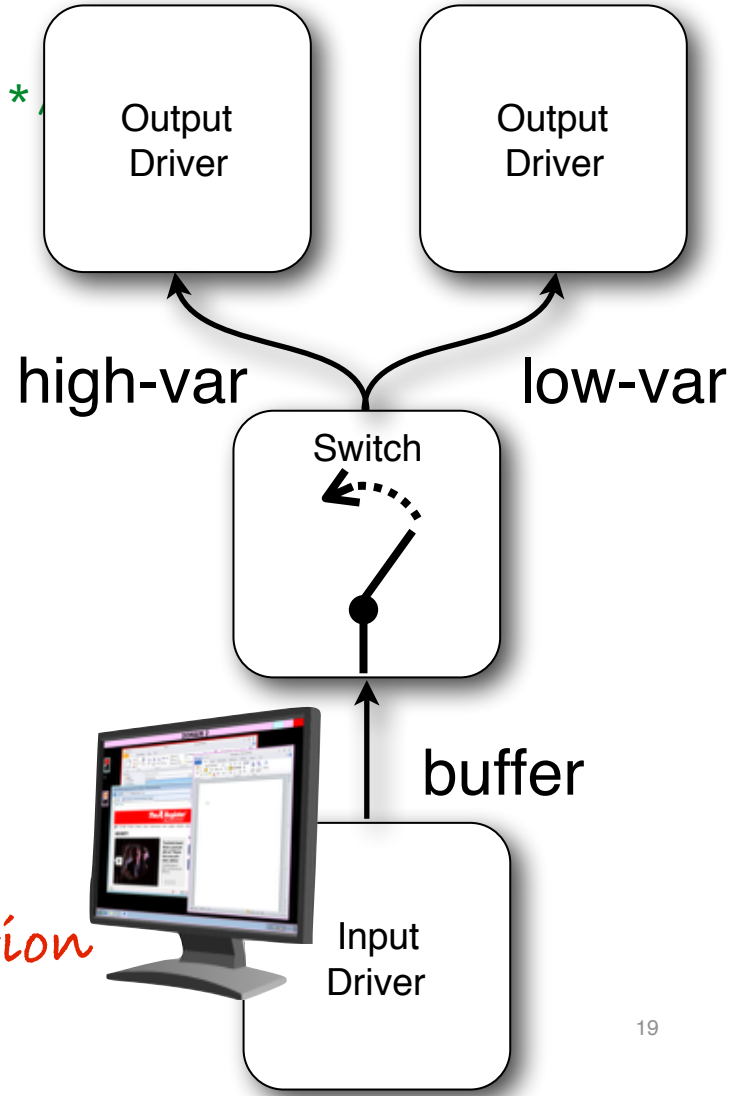

what if **dMode** and **sMode** disagree?



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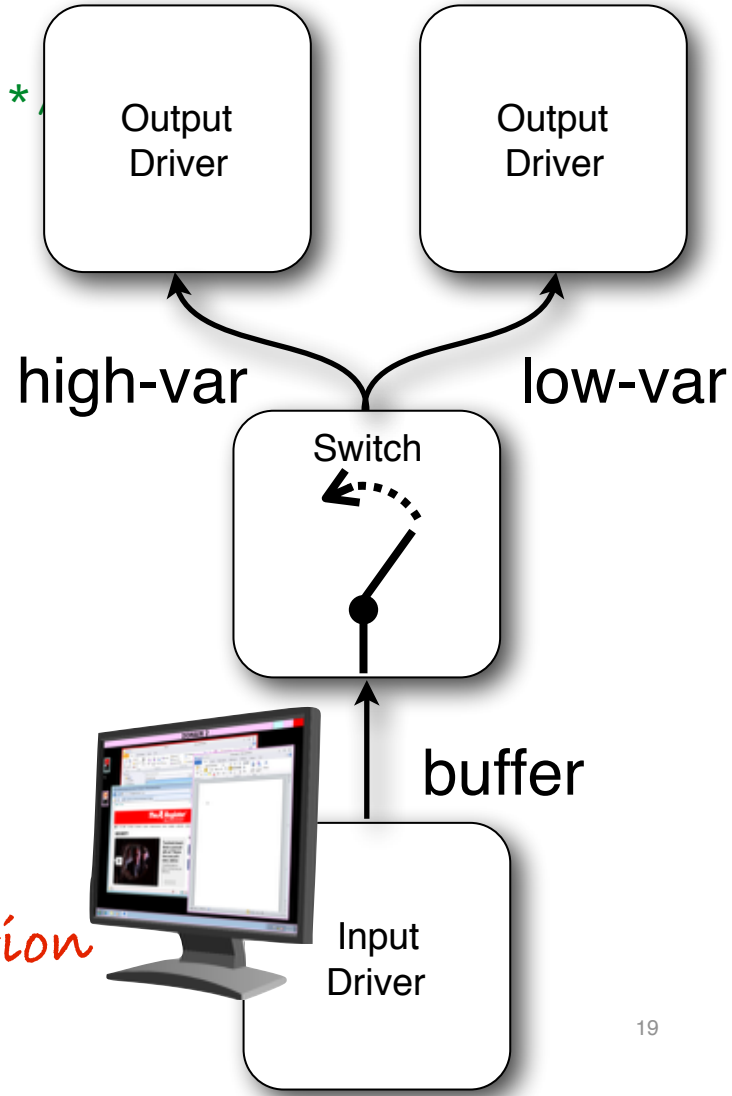

sMode *is switch's mode*

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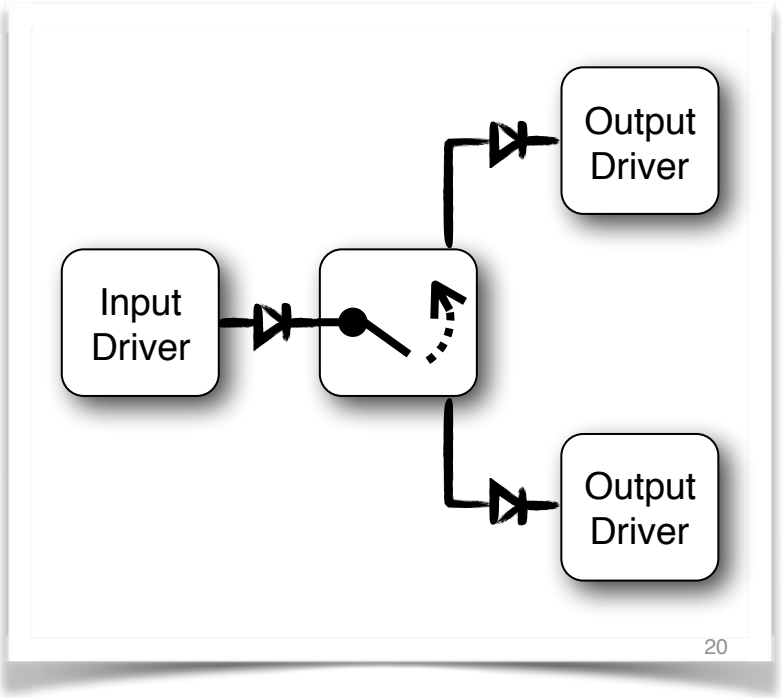
Verification Framework: Requirements

Verification Framework: Requirements

Compositional Security Property

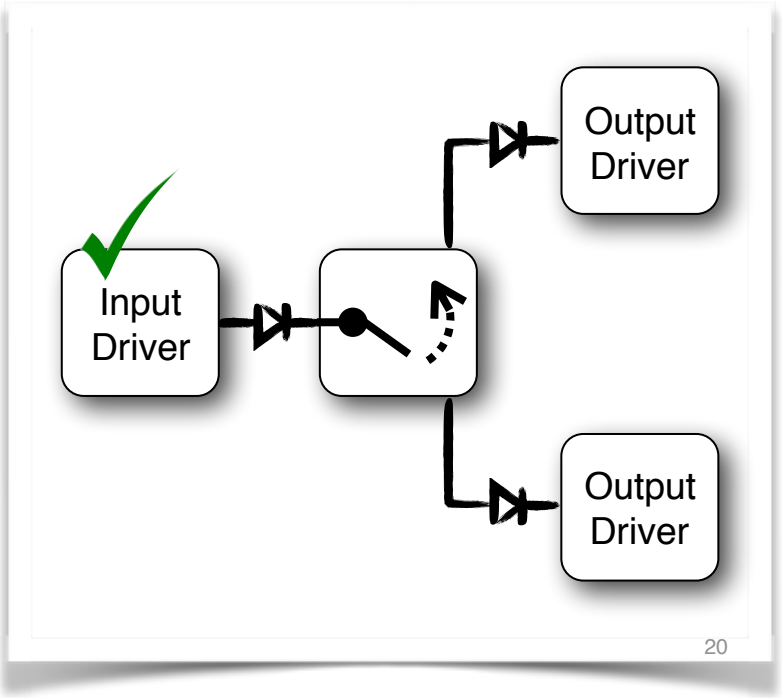
Verification Framework: Requirements

Compositional Security Property



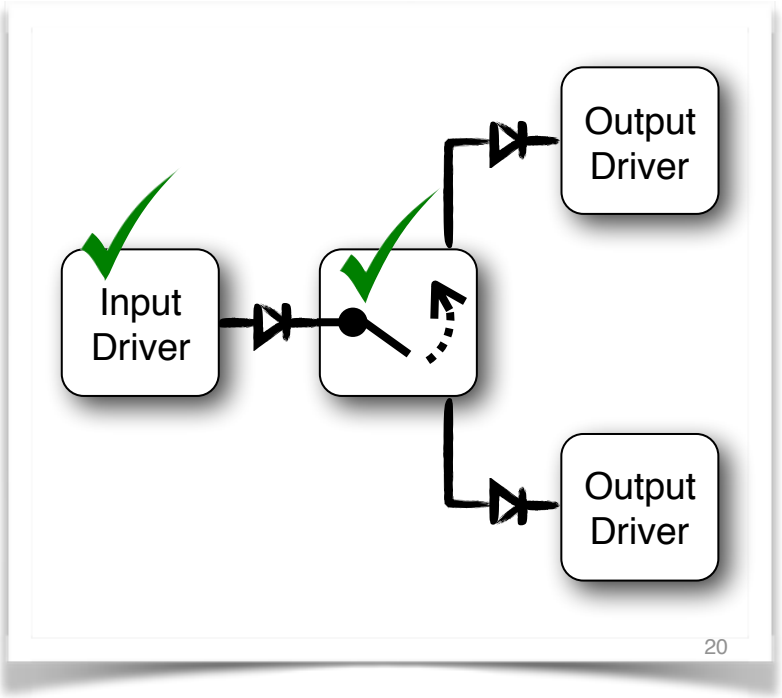
Verification Framework: Requirements

Compositional Security Property



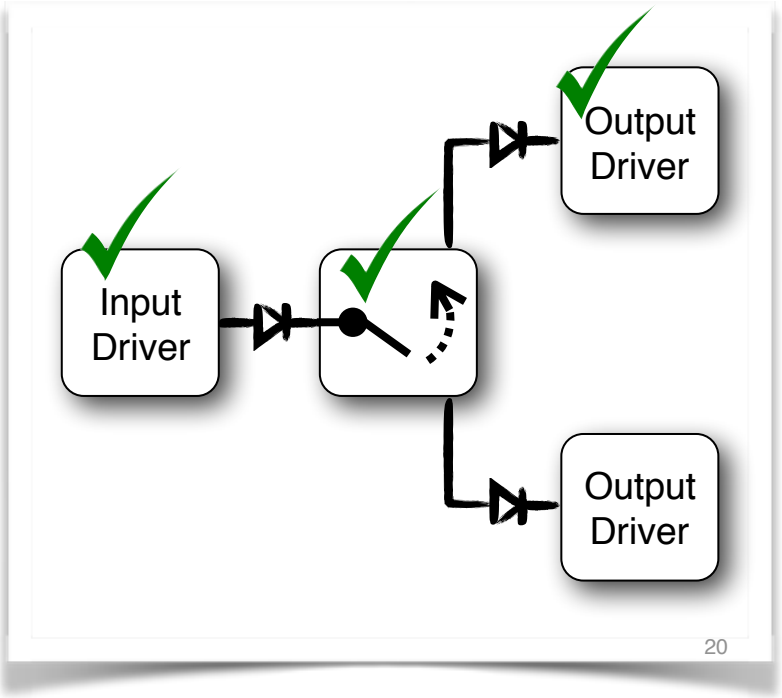
Verification Framework: Requirements

Compositional Security Property



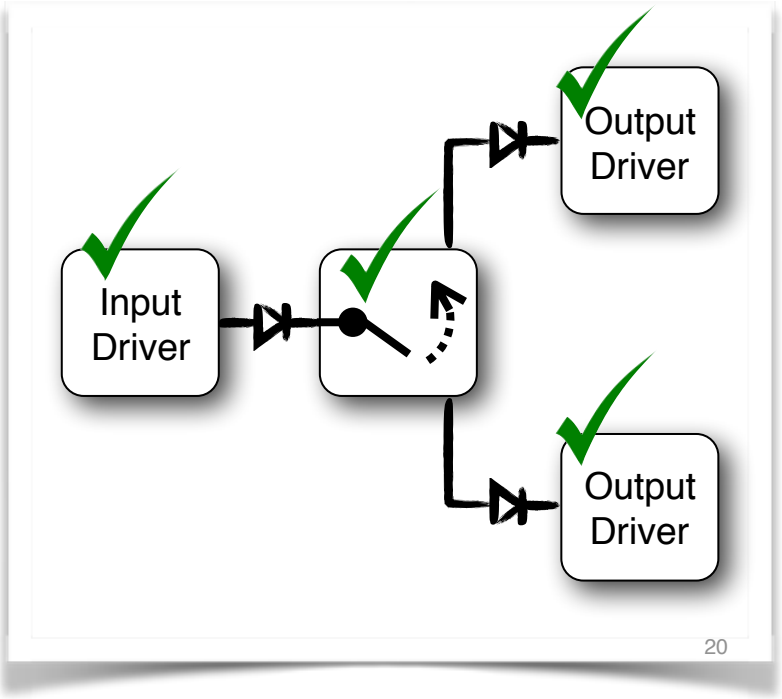
Verification Framework: Requirements

Compositional Security Property



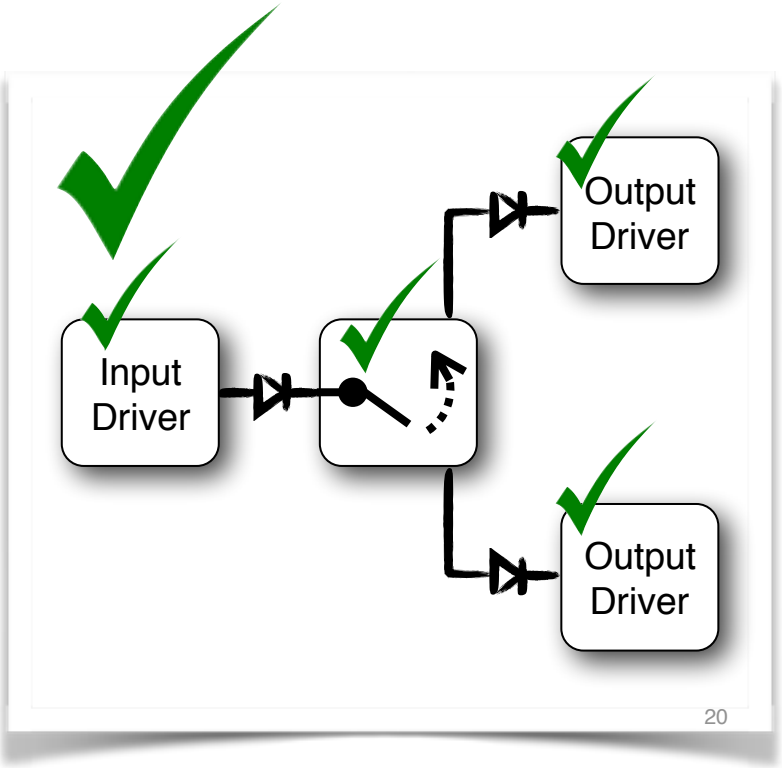
Verification Framework: Requirements

Compositional Security Property



Verification Framework: Requirements

Compositional Security Property



Verification Framework: Requirements

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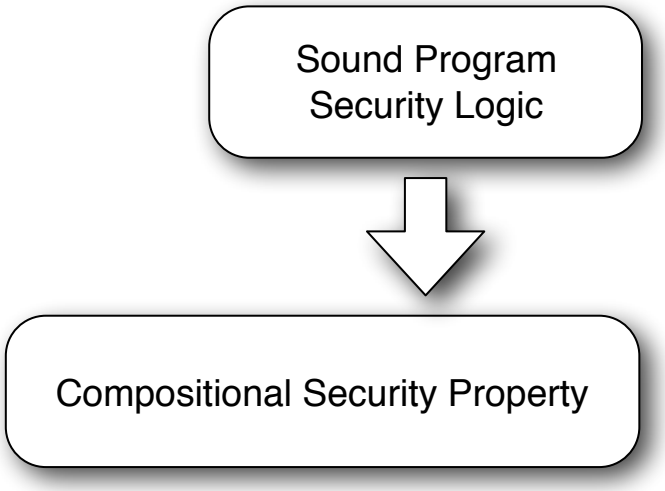
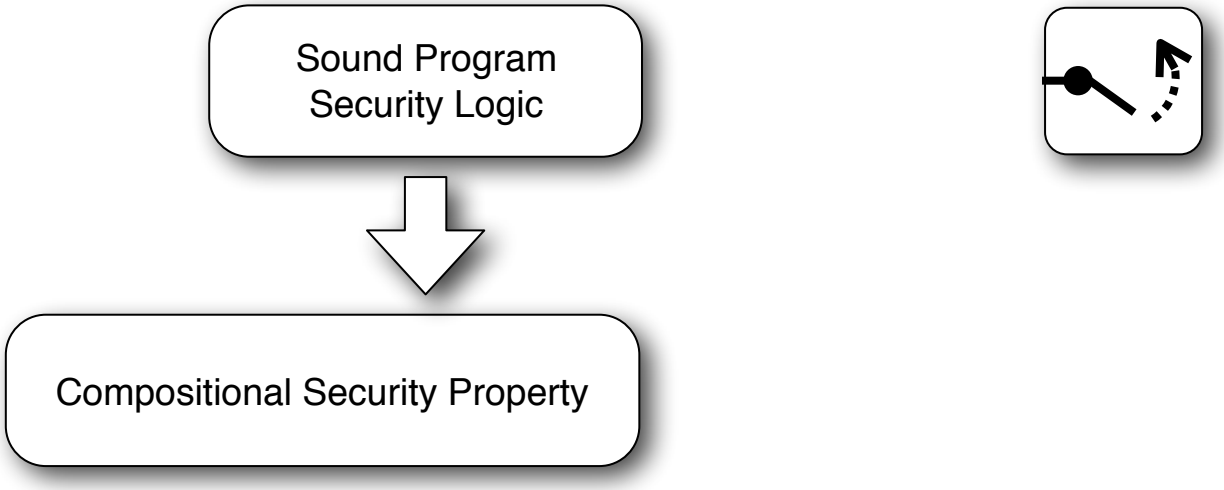
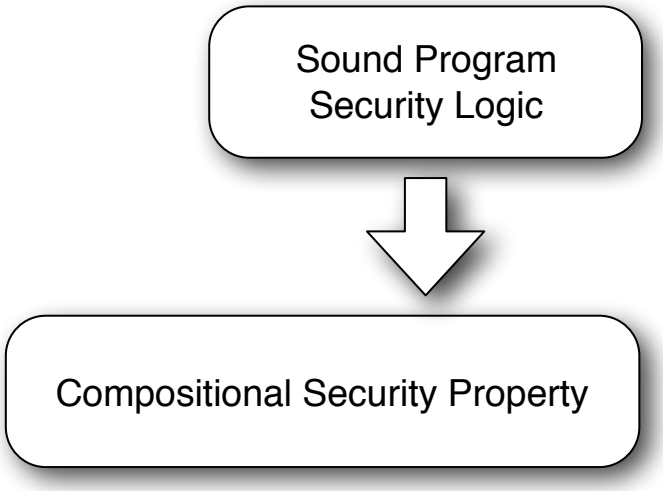


Verification Framework: Requirements

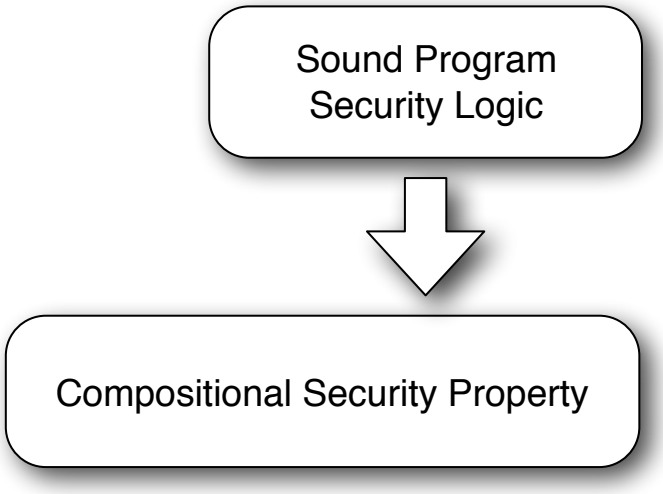


Verification Framework: Requirements




```
skip   /* control +=_m AsmNoW */;
skip   /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
  low-var := temp
else
  high-var := temp
endif;
temp := 0;
skip   /* temp -=_m AsmNoRW */
```

Verification Framework: Requirements

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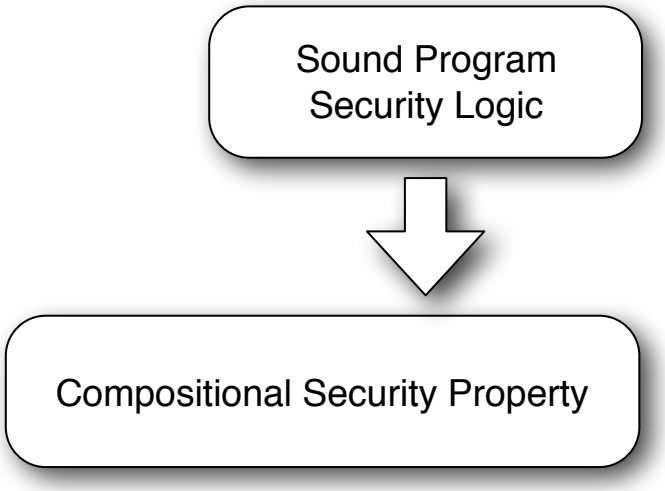

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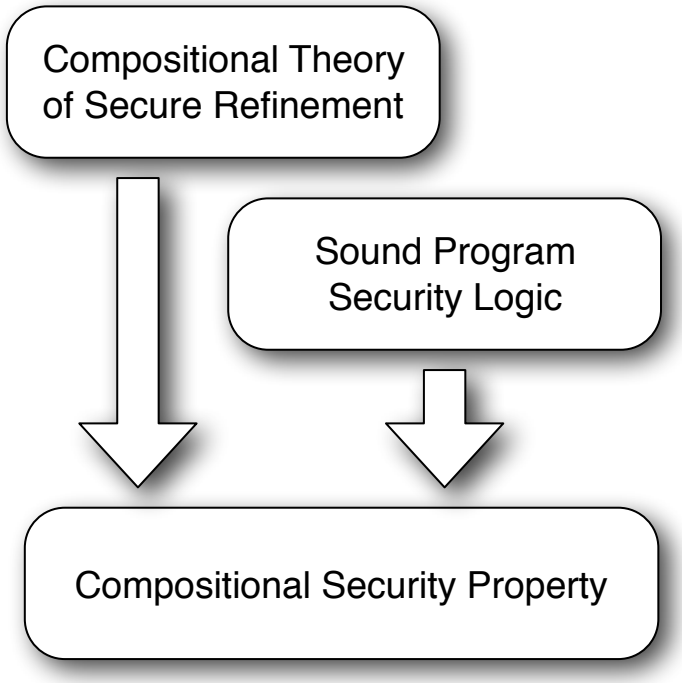

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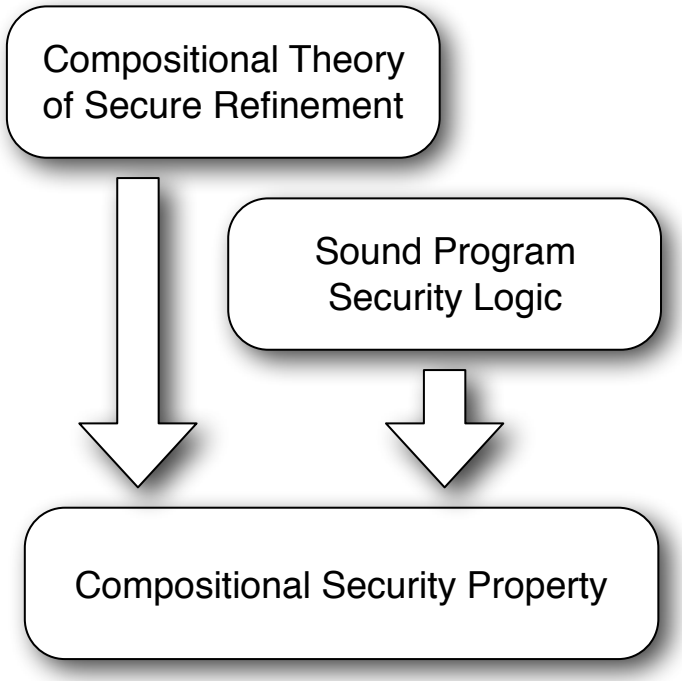
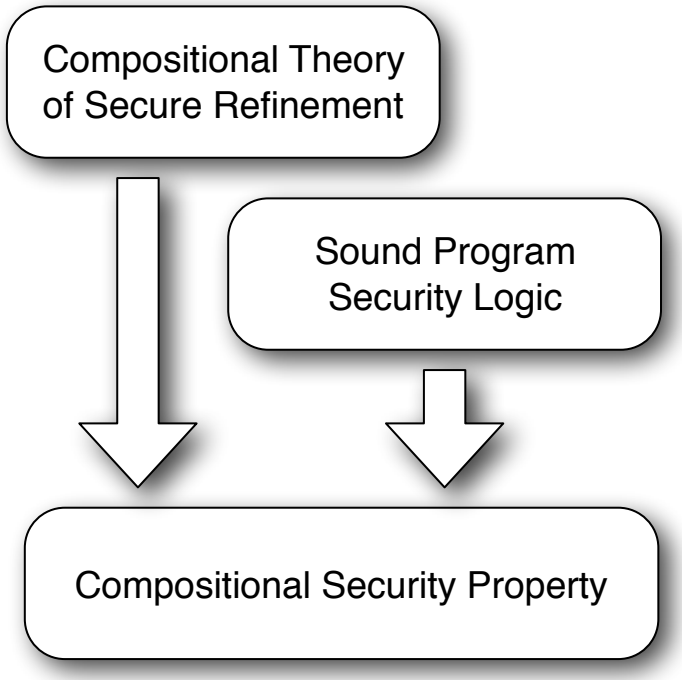
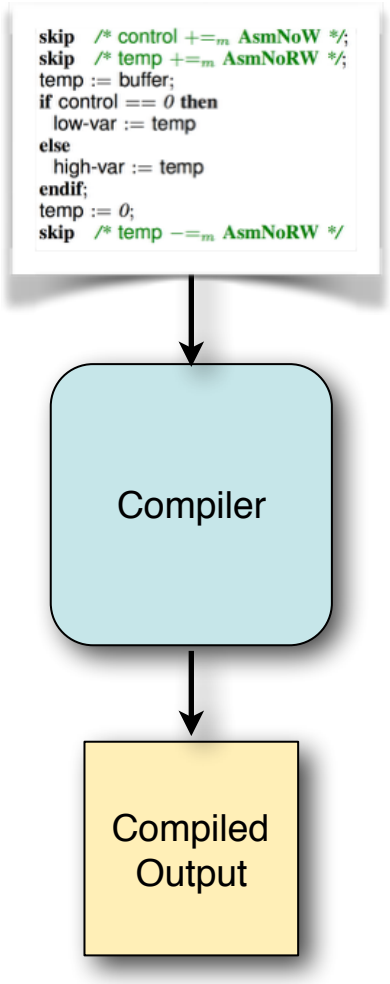
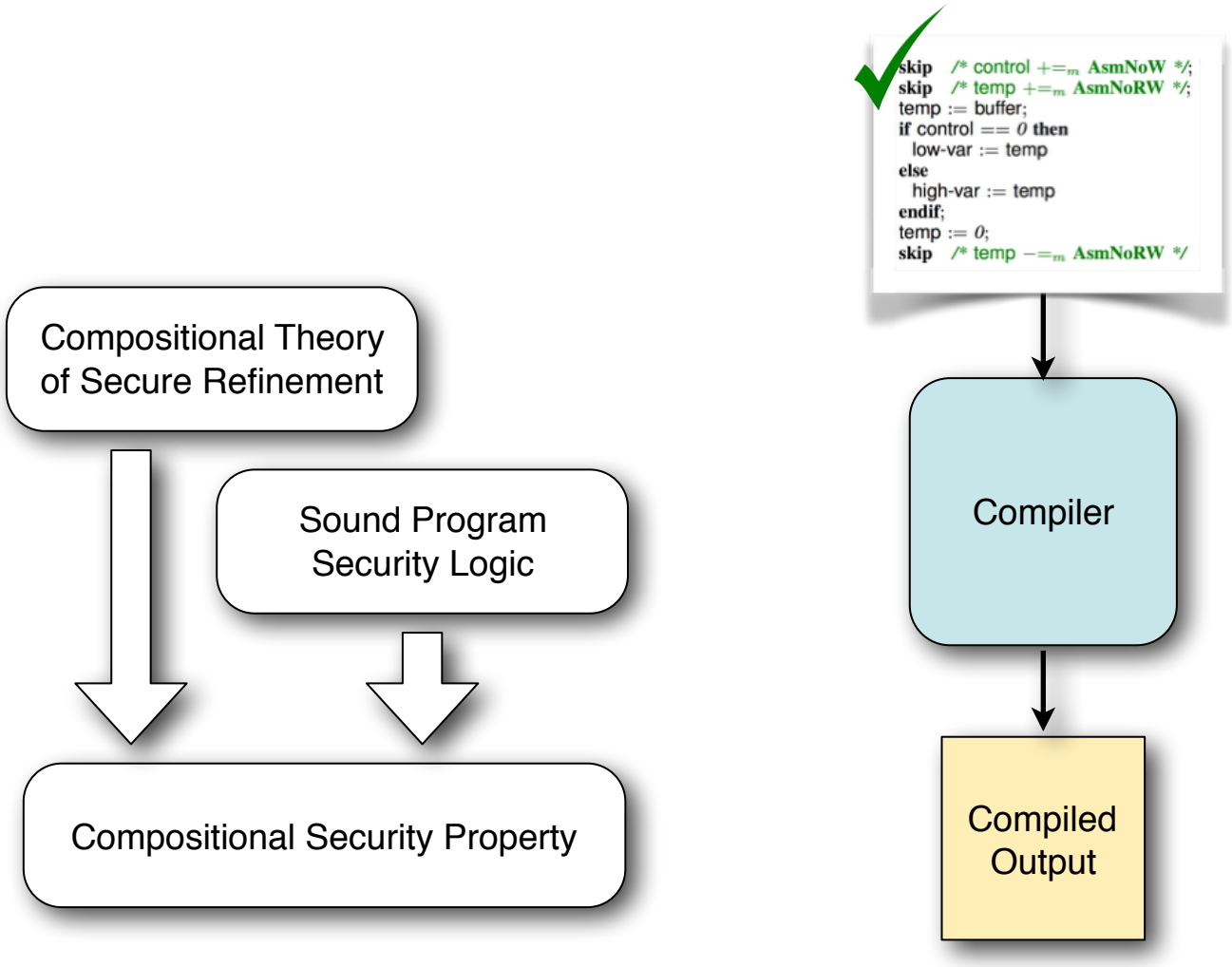


Verification Framework: Requirements

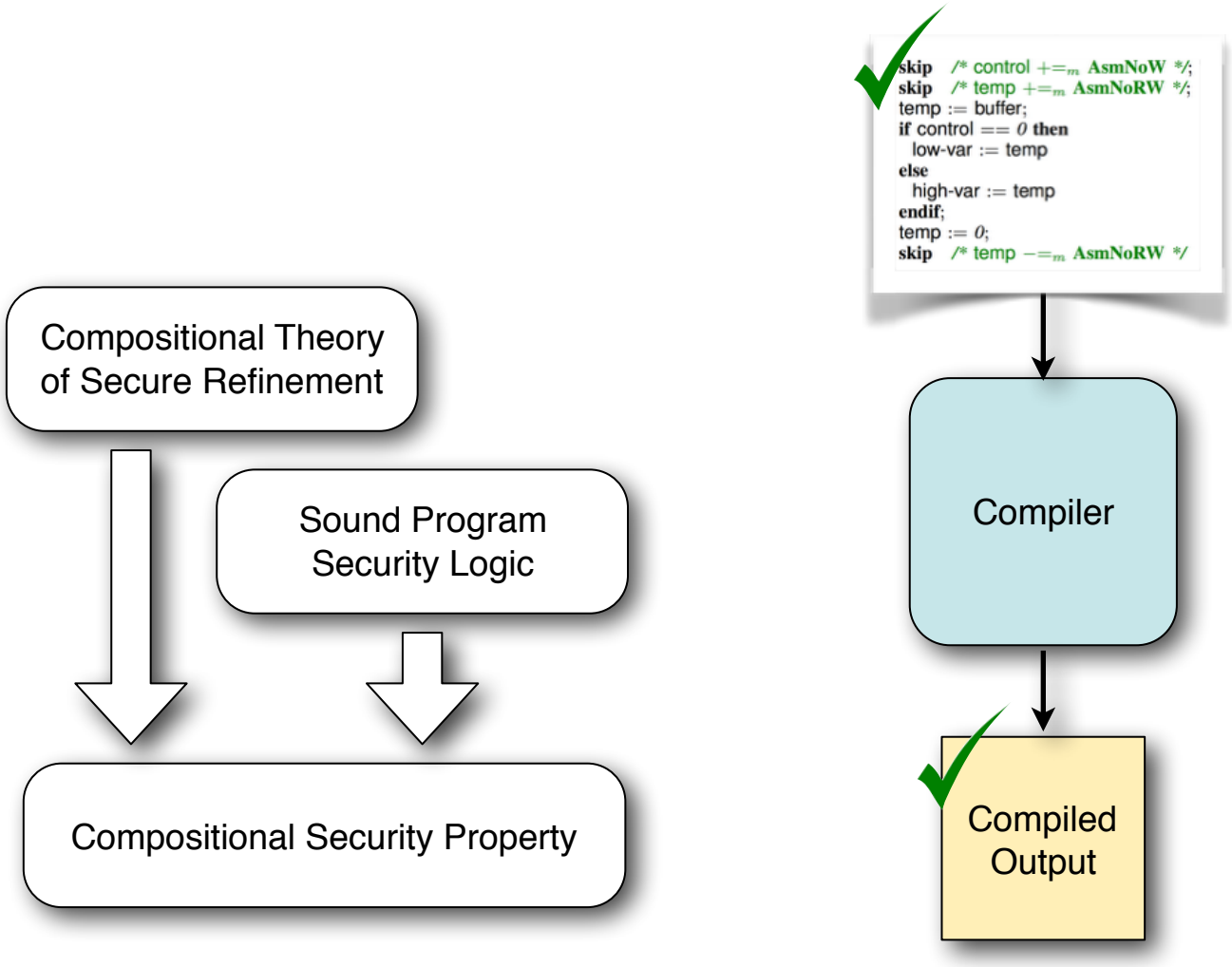




Verification Framework: Requirements



Verification Framework: Requirements



Verification Framework: Operation

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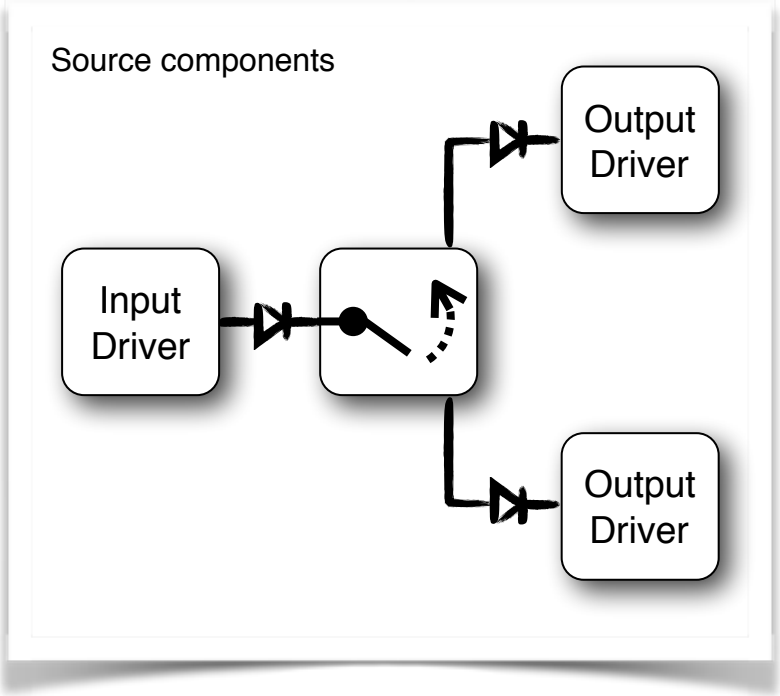
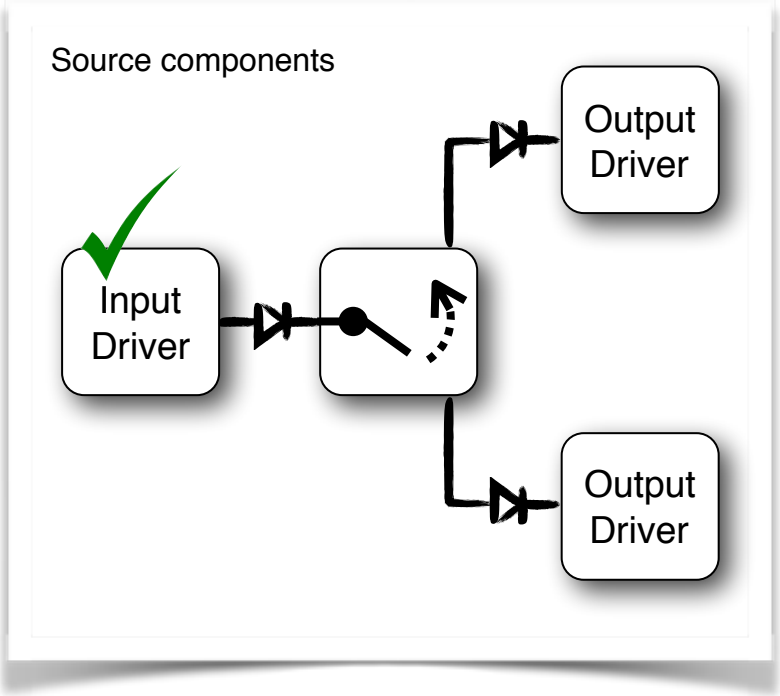


Verification Framework: Operation



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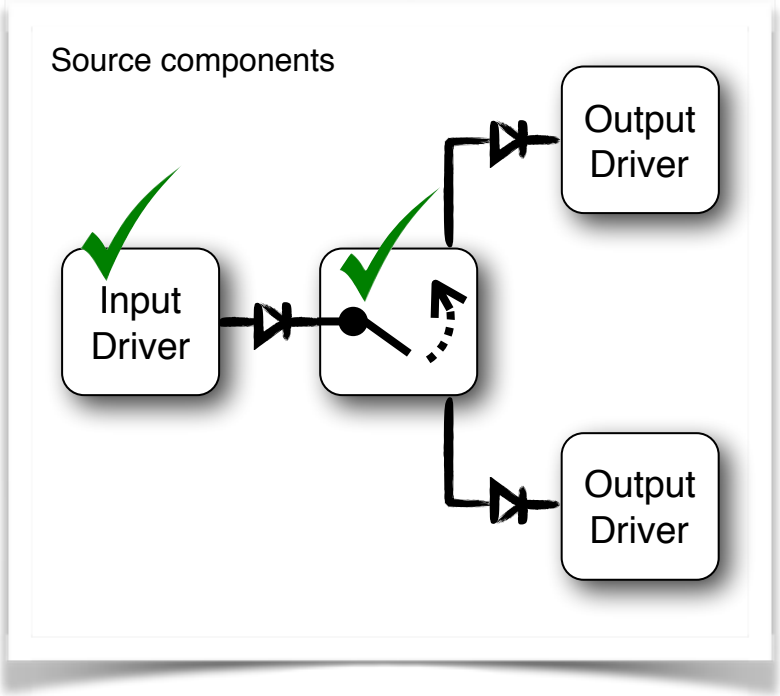

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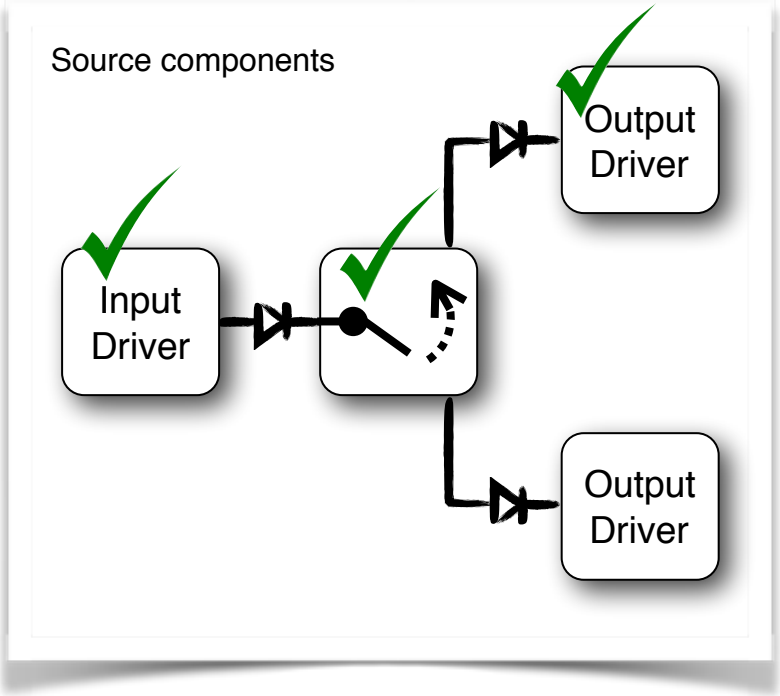

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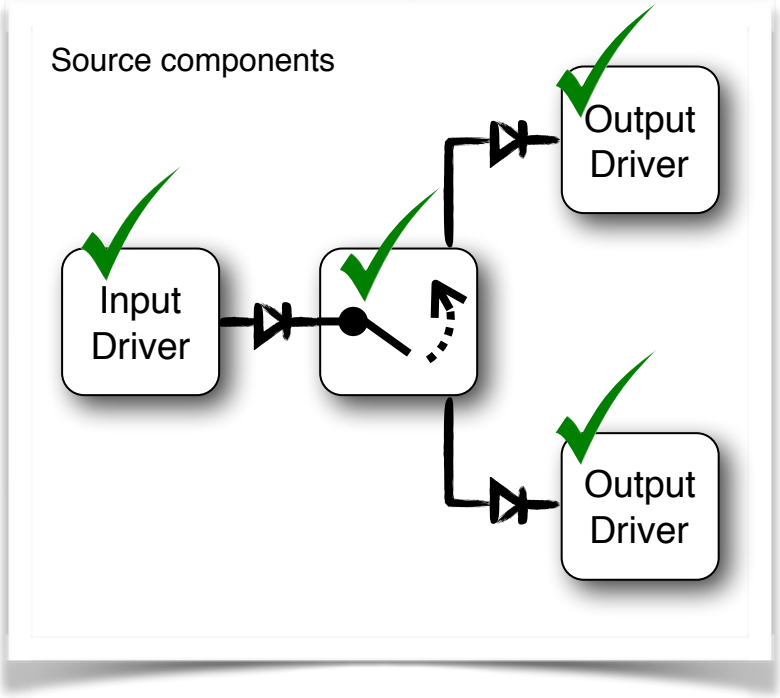

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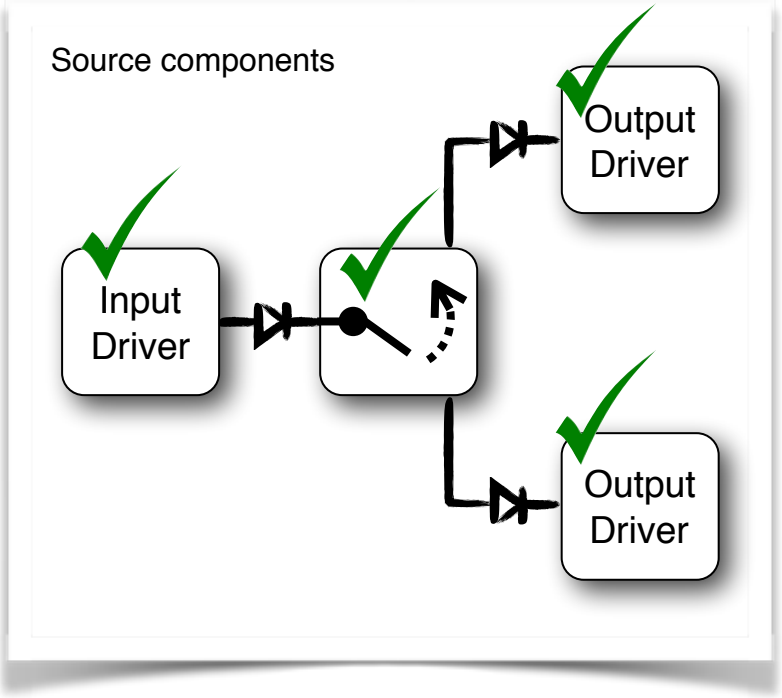
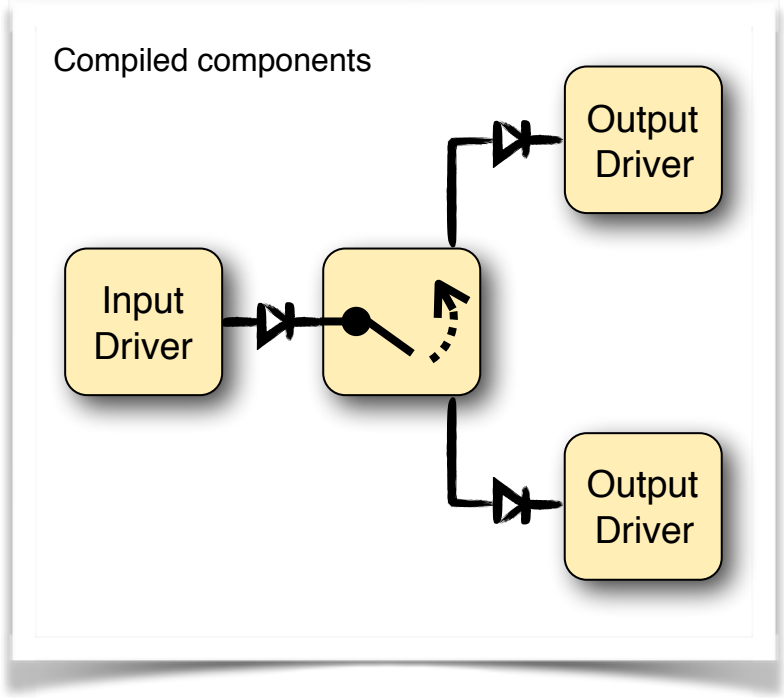
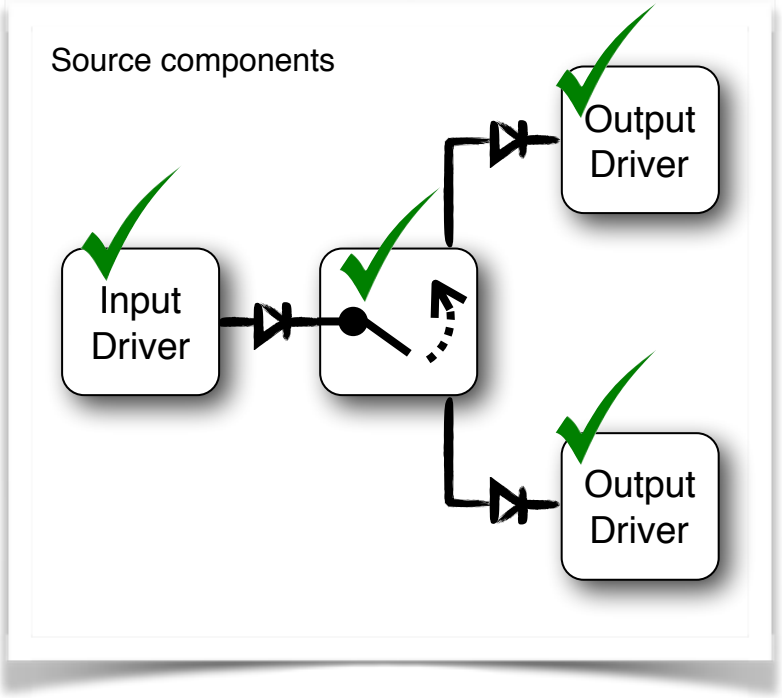
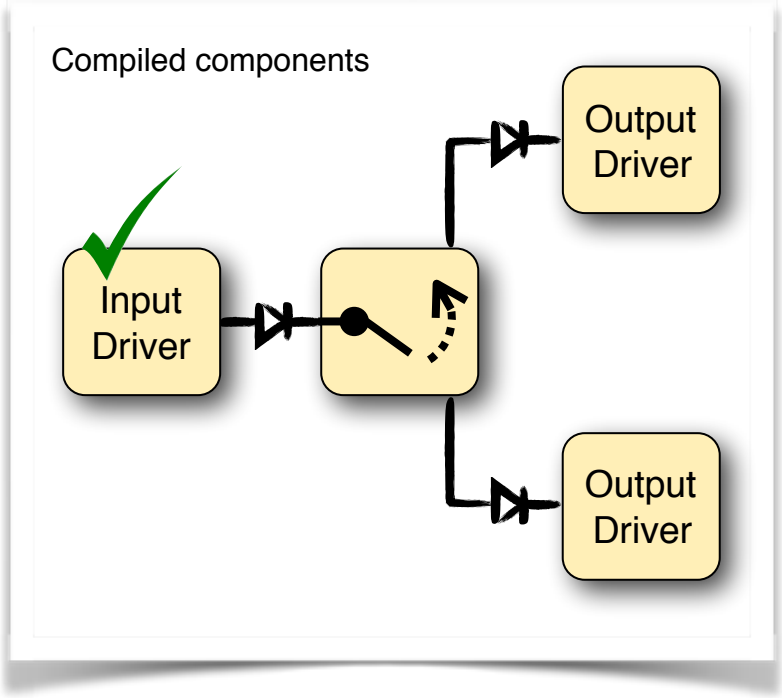


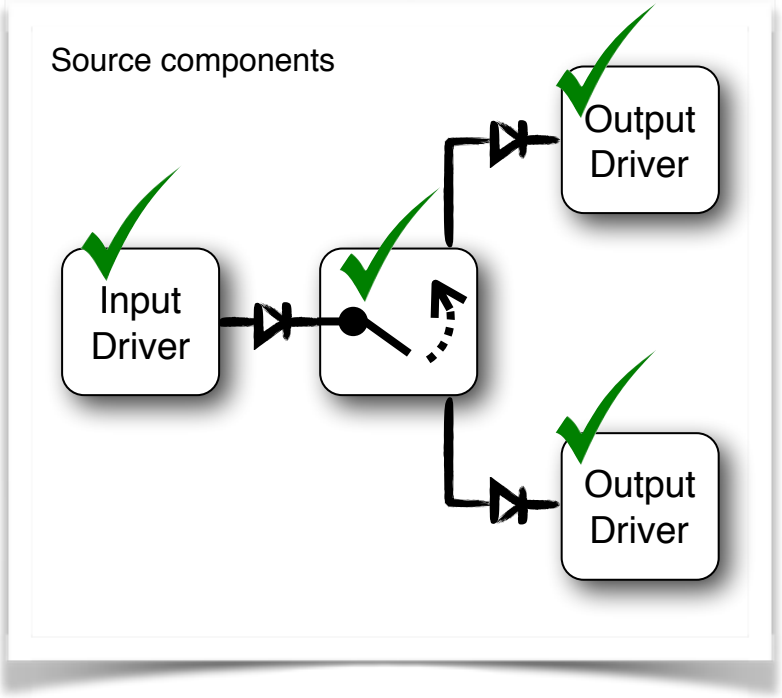


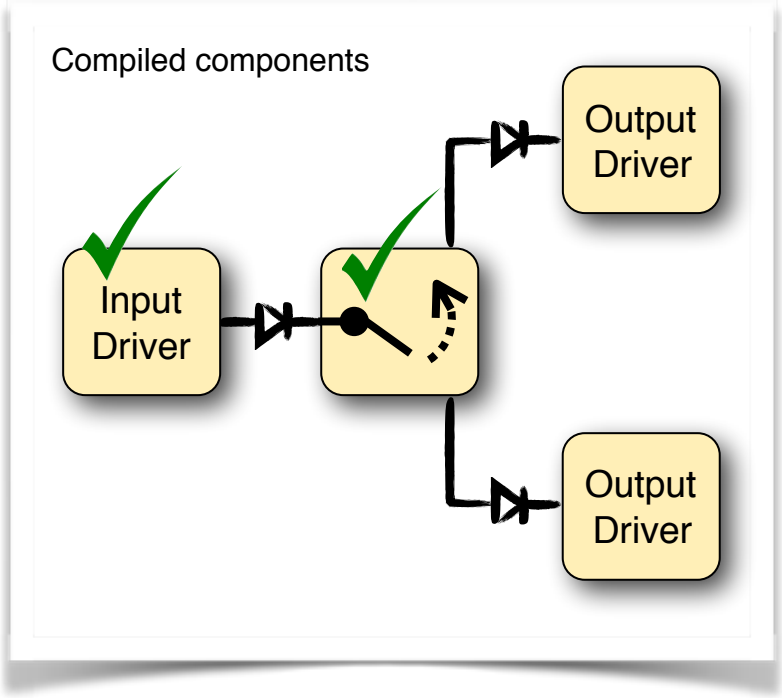
Verification Framework: Operation



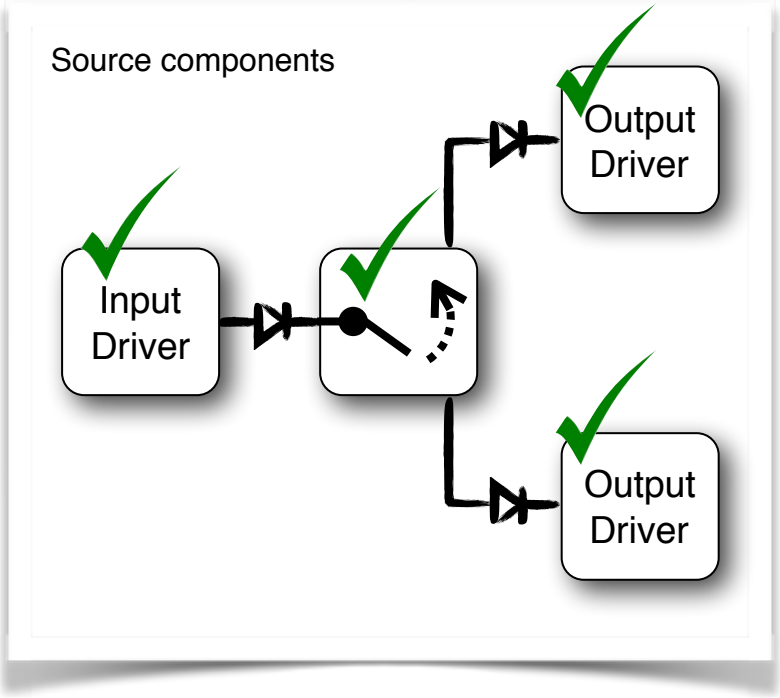


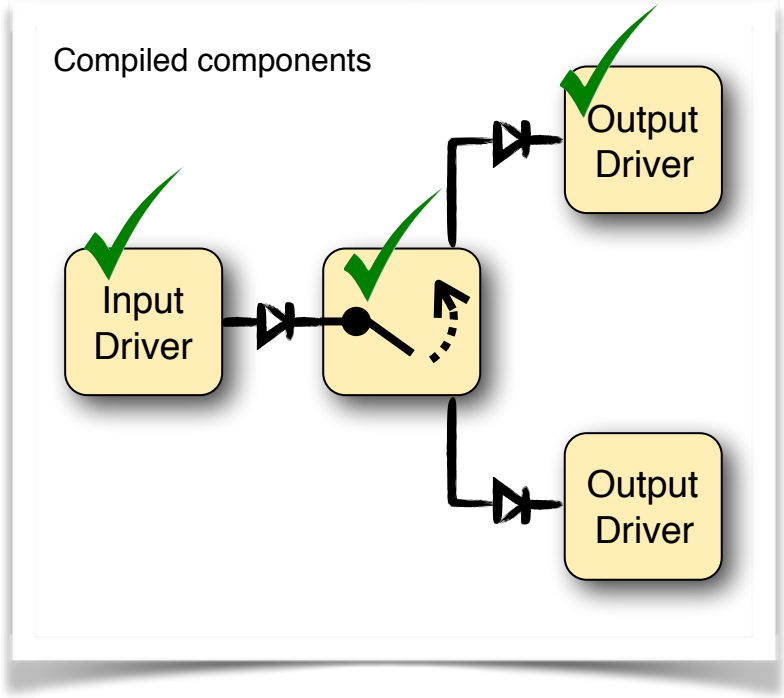
Verification Framework: Operation





Verification Framework: Operation





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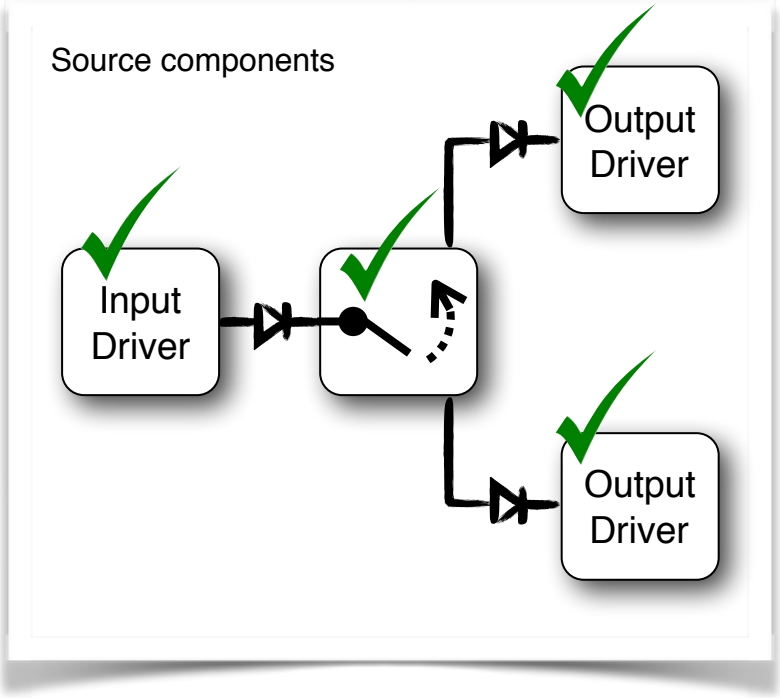

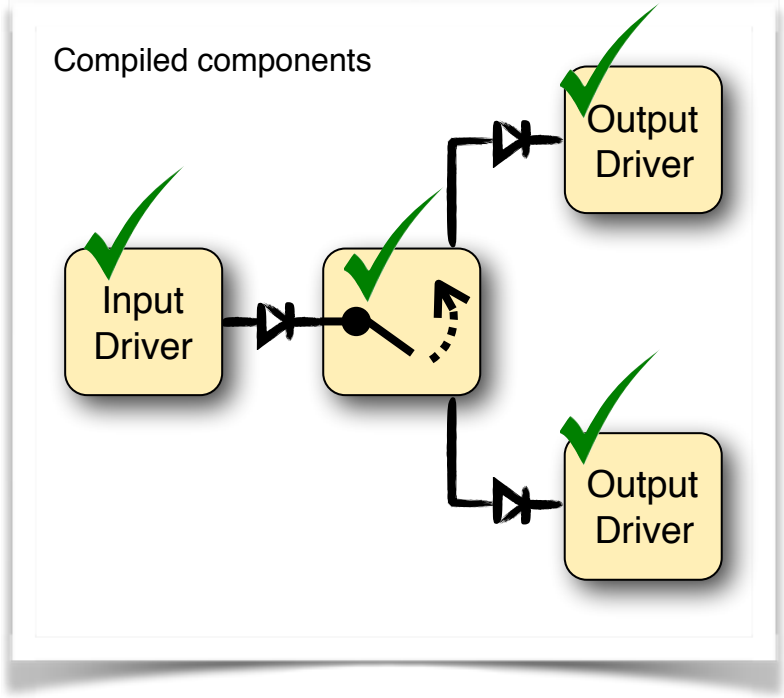

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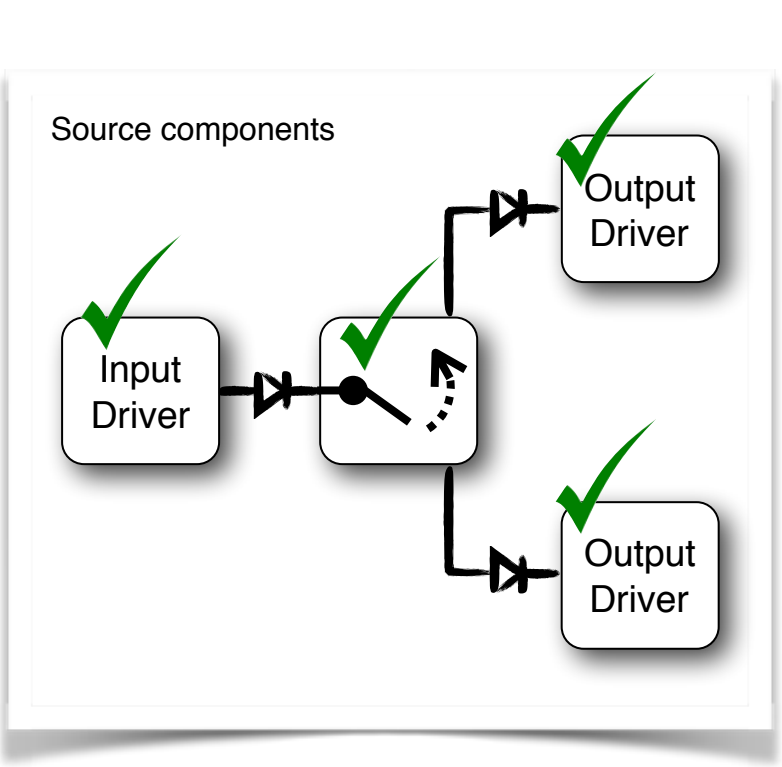
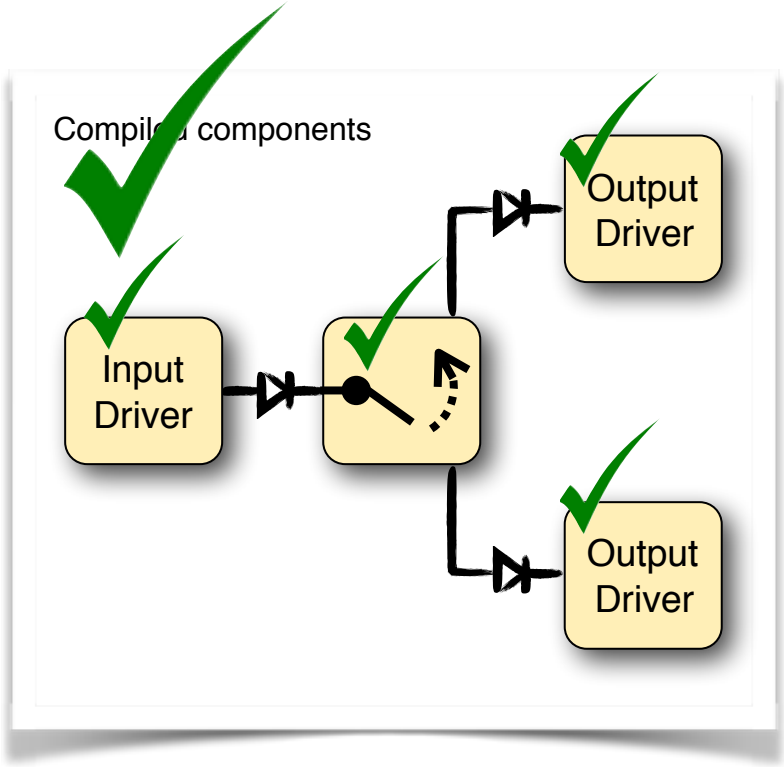
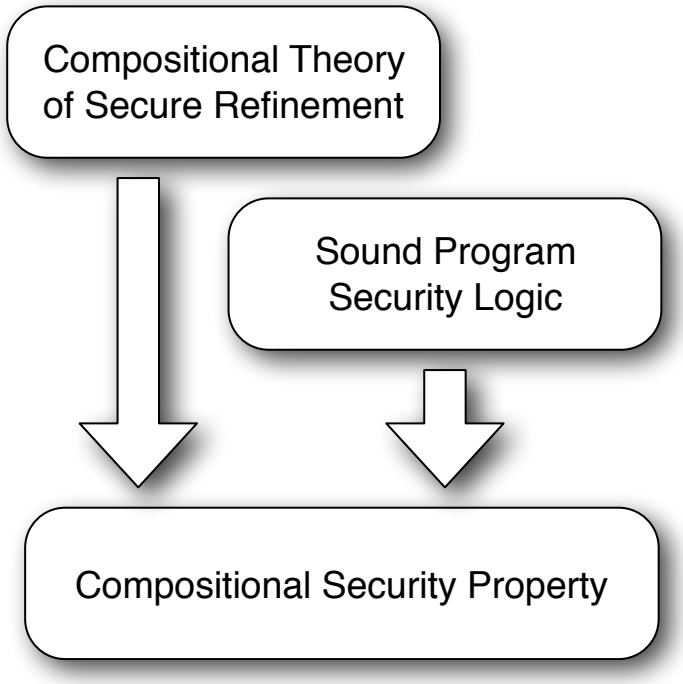
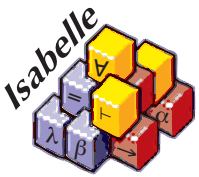


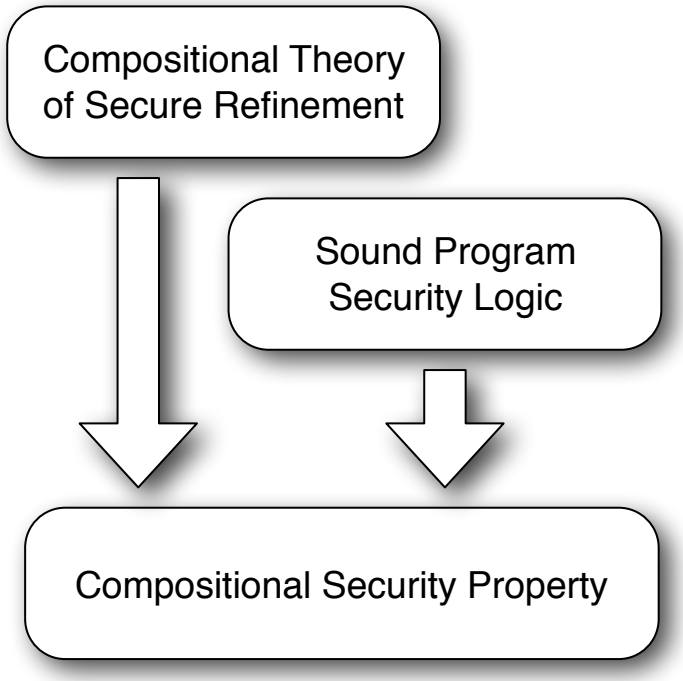


Verification Framework: Status



Verification Framework: Status





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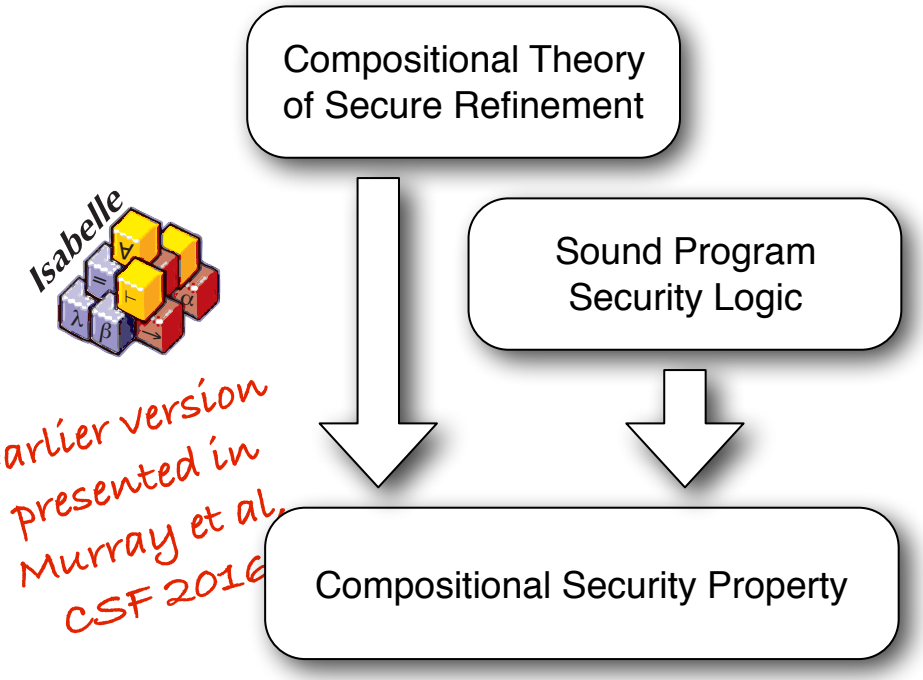
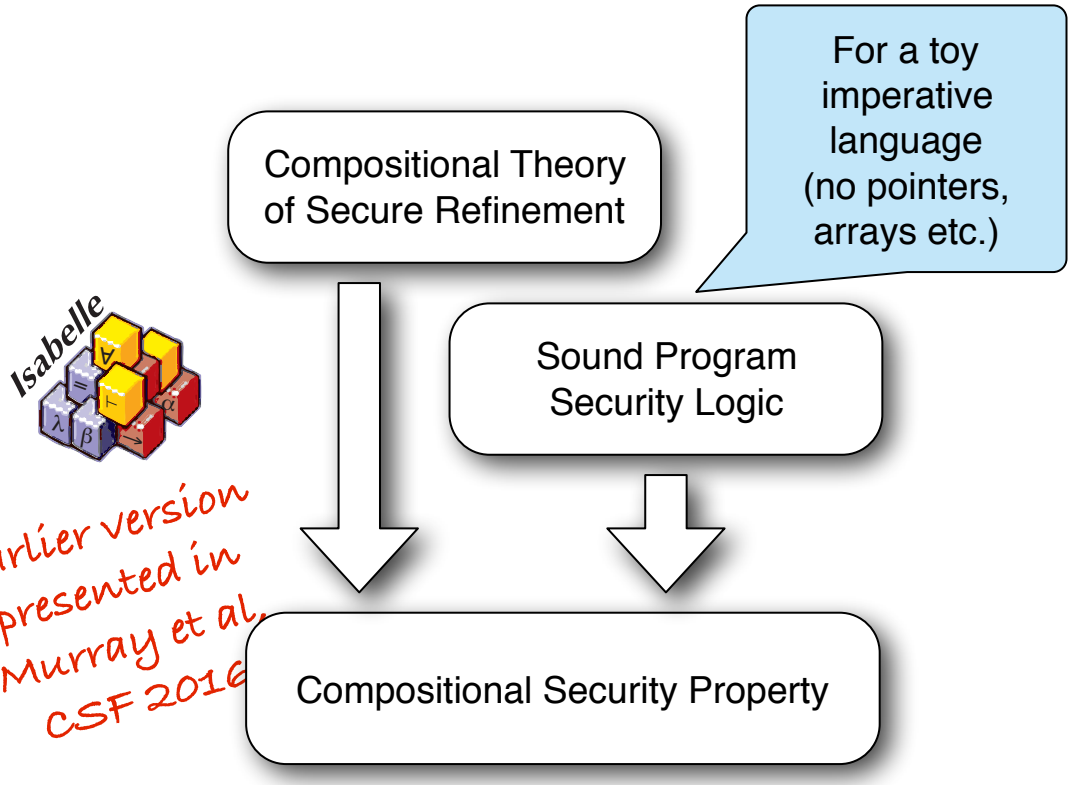
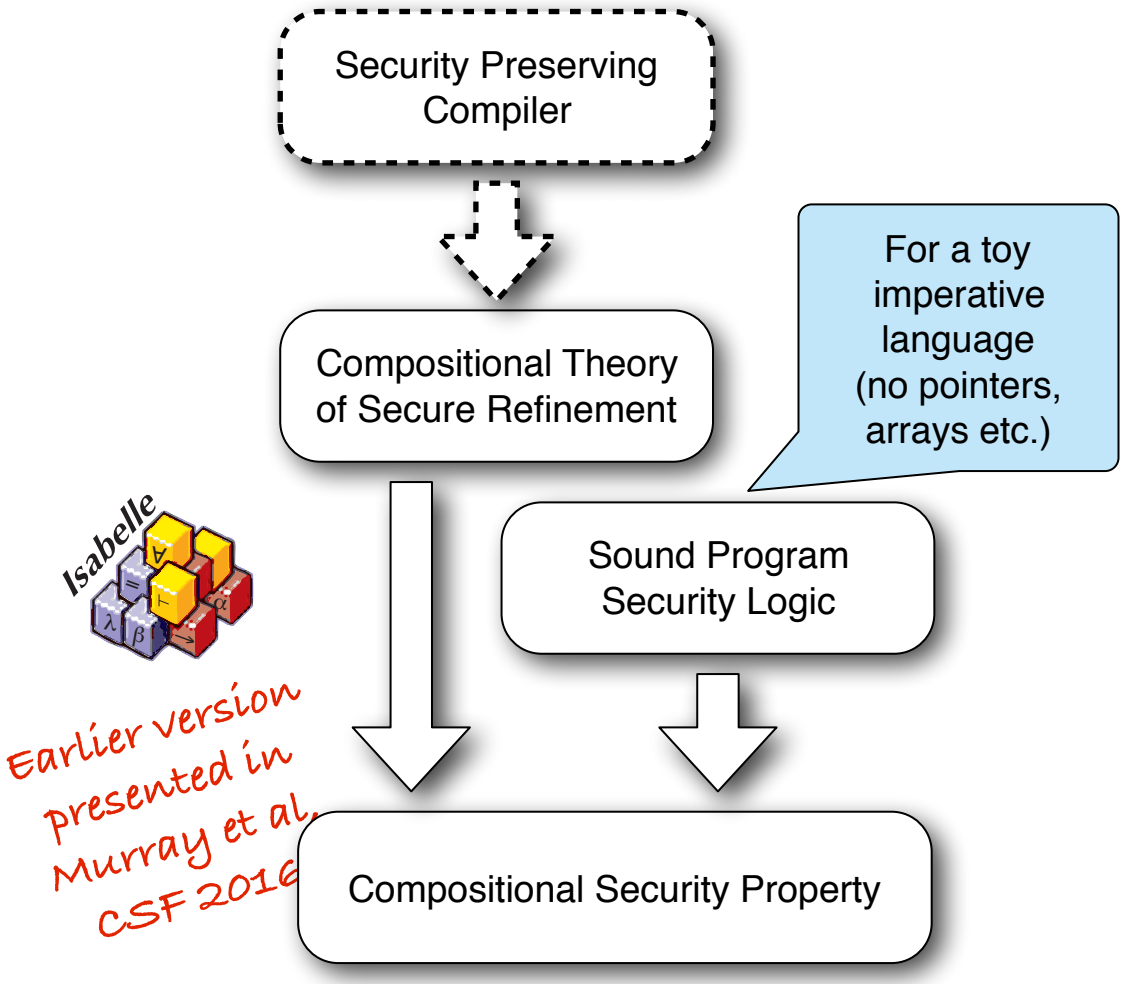


Verification Framework: Status

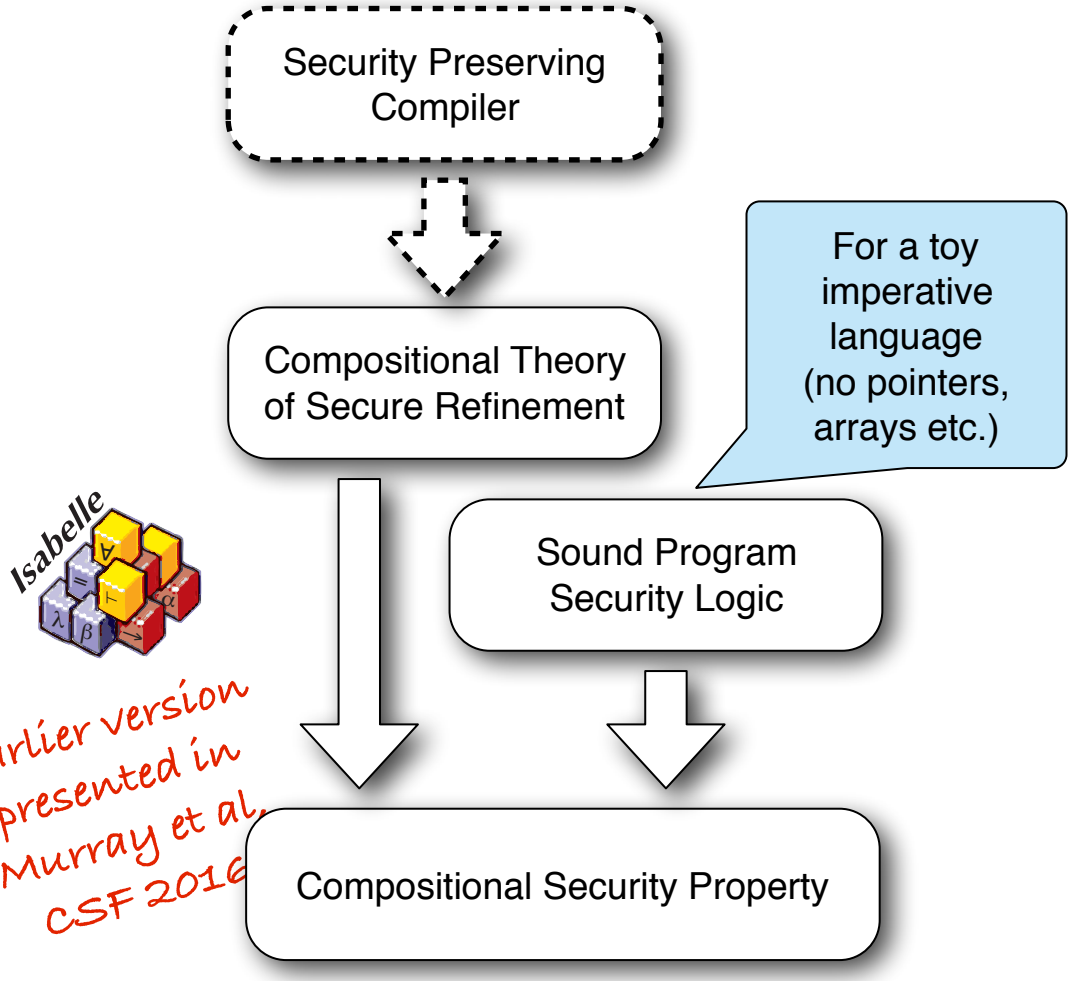


Verification Framework: Status

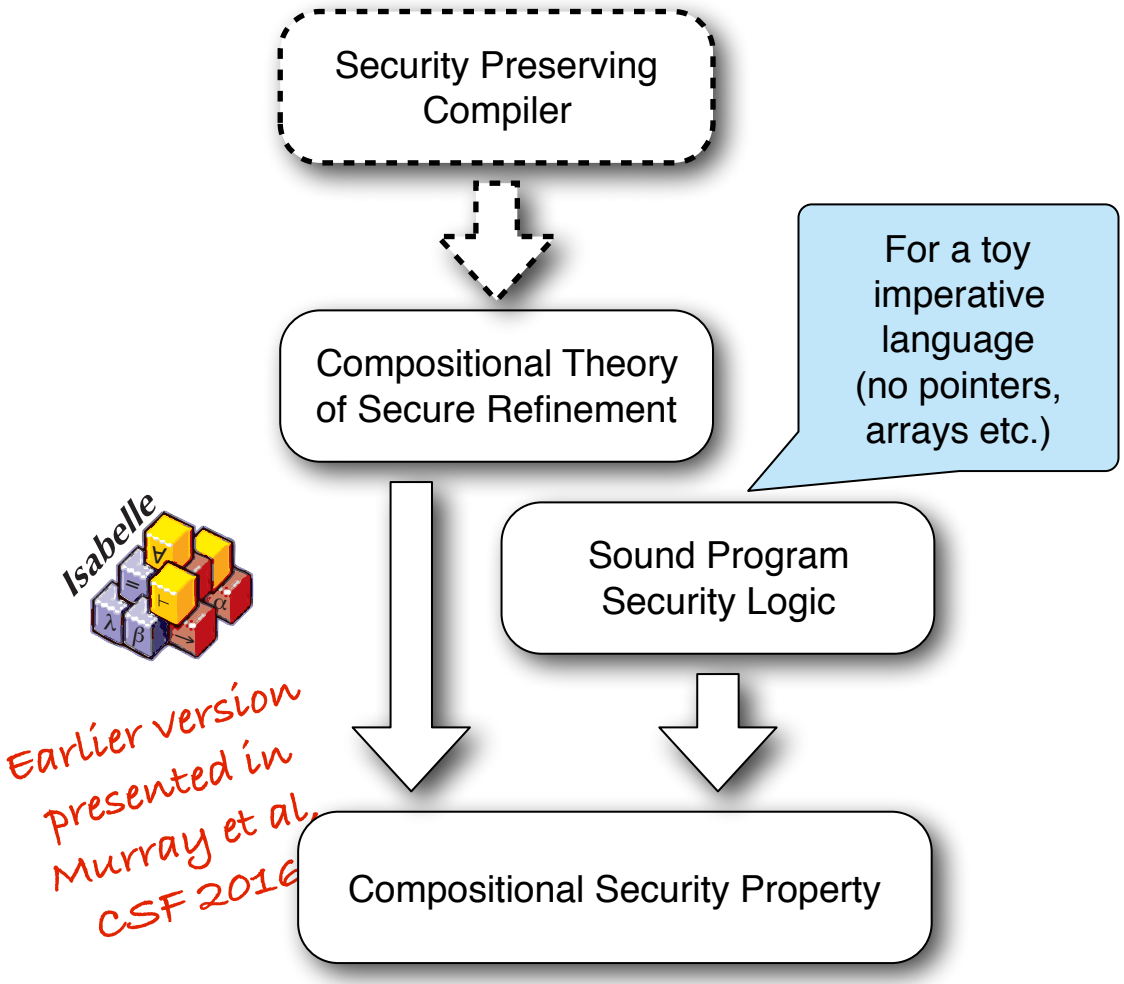


Verification Framework: Status

Robert Sison



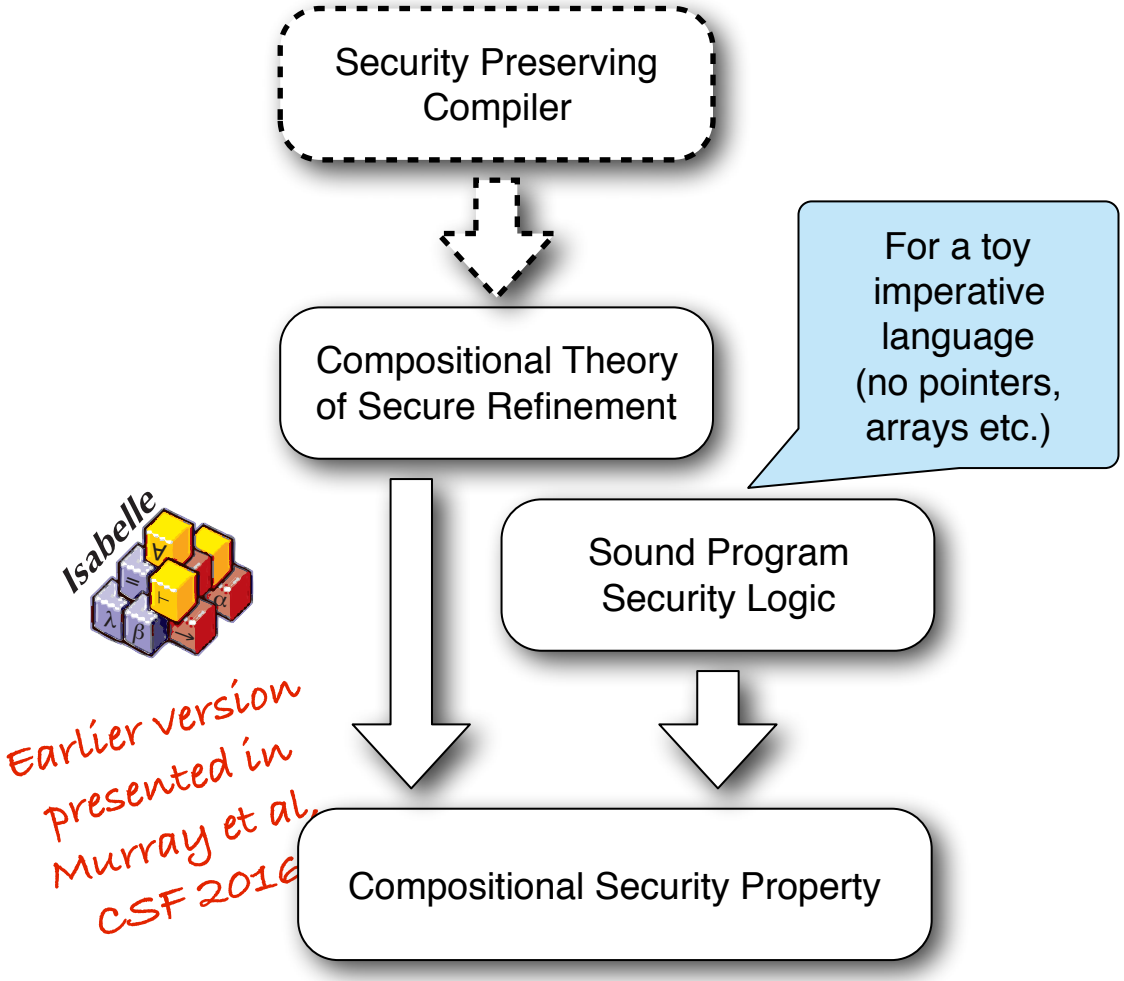
Verification Framework: Status



Robert Sison

Edward Pierzchalski

Verification Framework: Status

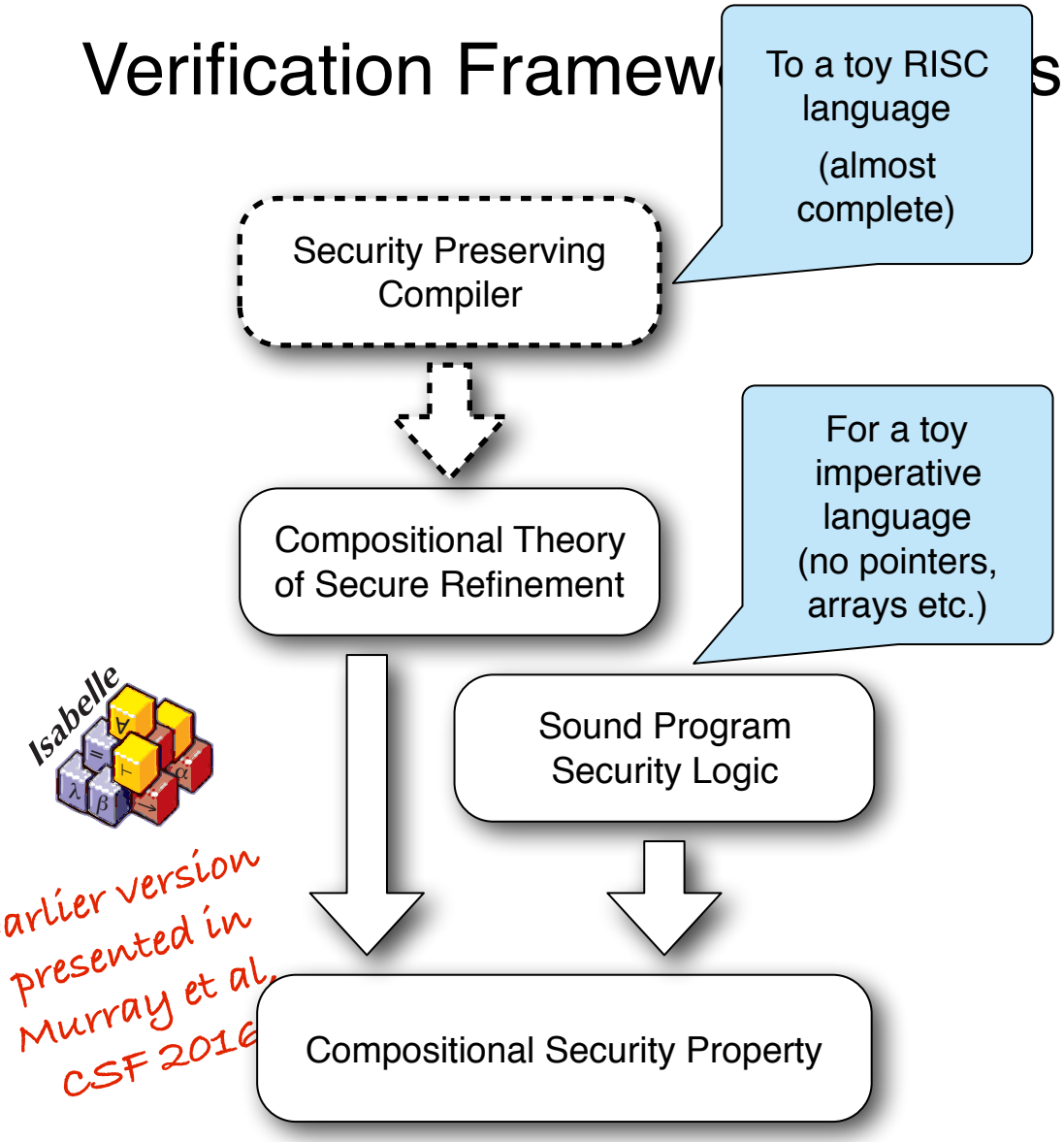


Robert Sison

Edward Pierzchalski

Christine Rizkallah

Verification Framew s

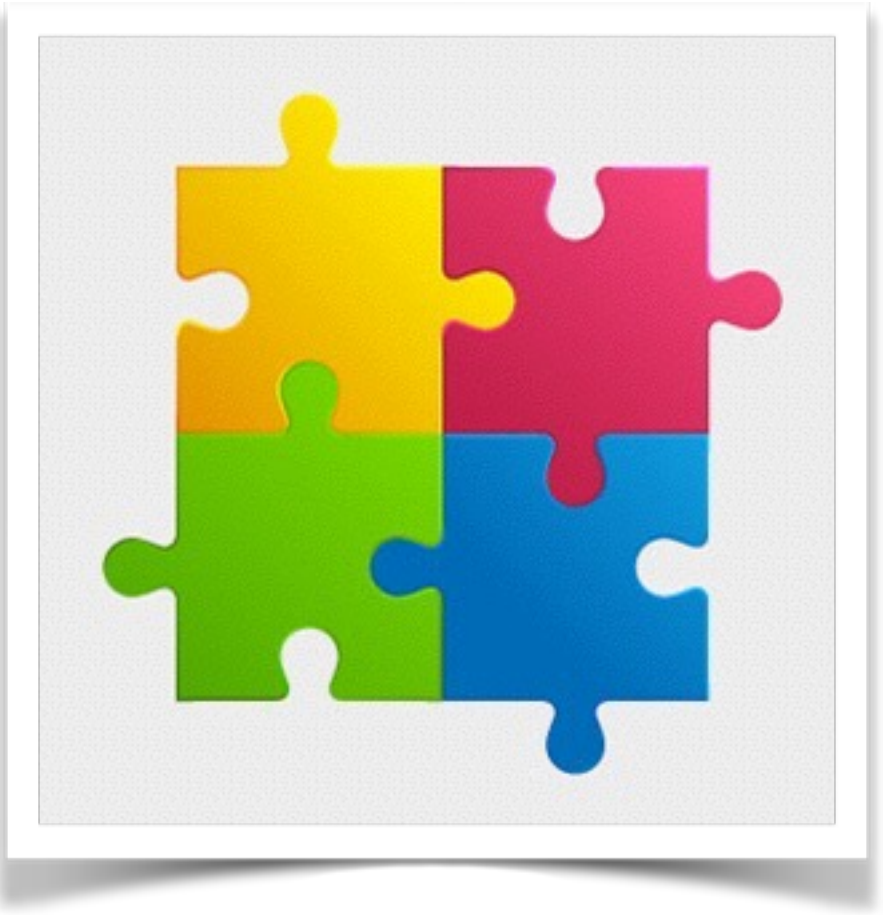


Robert Sison

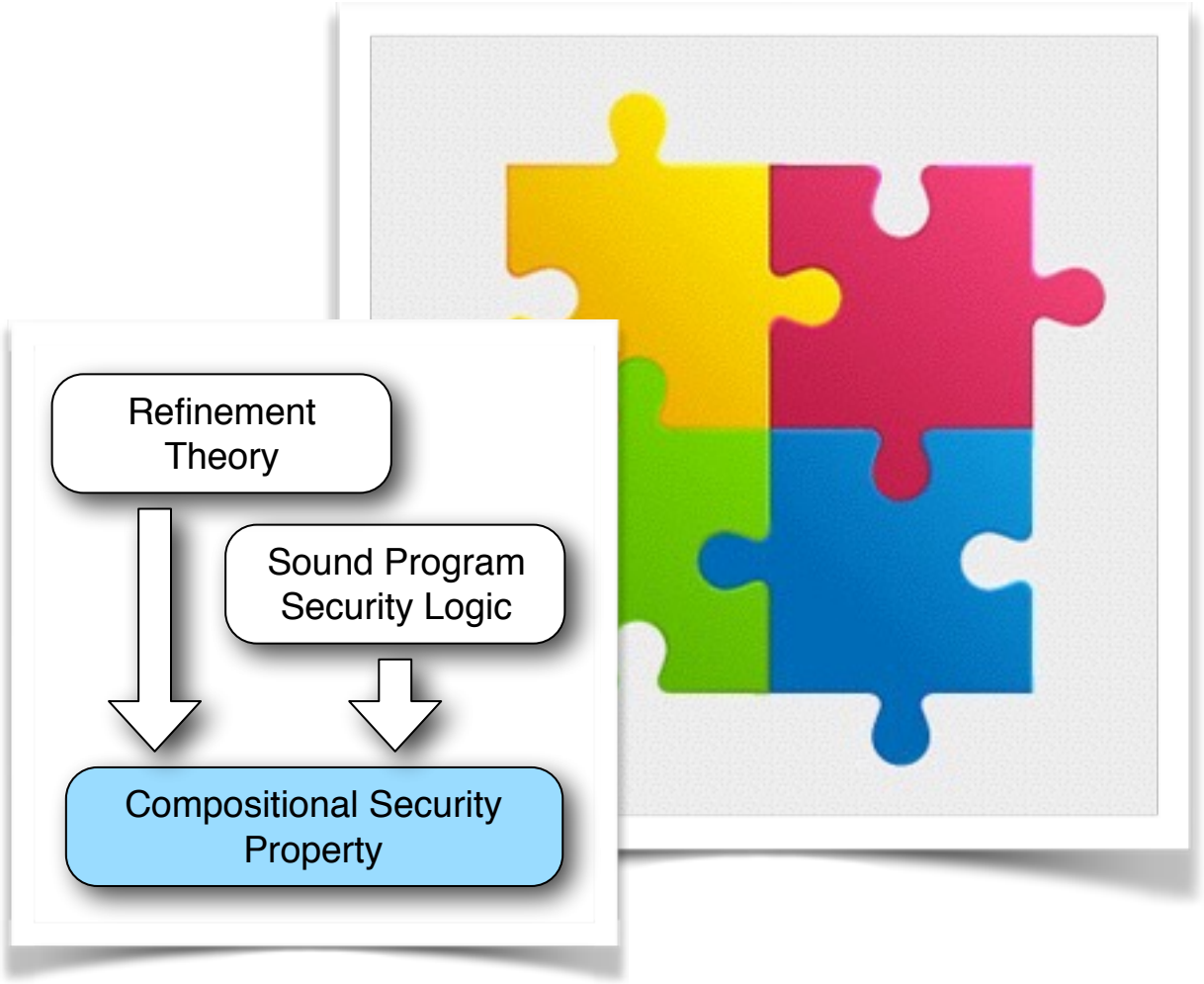
Edward Pierzchalski

Christine Rizkallah

COMPOSITIONAL SECURITY



COMPOSITIONAL SECURITY



Minimum Requirements

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if (h){
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l = 1;
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Secure?

Minimum Requirements

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Secure?

Timing-Insensitive Security:

Minimum Requirements

```
l = 0;
if (h){
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l = 1;
```

Secure?

Timing-Insensitive Security: **YES**

Minimum Requirements

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l = 0;
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Secure?

Timing-Insensitive Security: **YES**

Timing-Sensitive Security:

Minimum Requirements

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Secure?

Timing-Insensitive Security: **YES**

Timing-Sensitive Security: **NO**

Minimum Requirements

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print(l);
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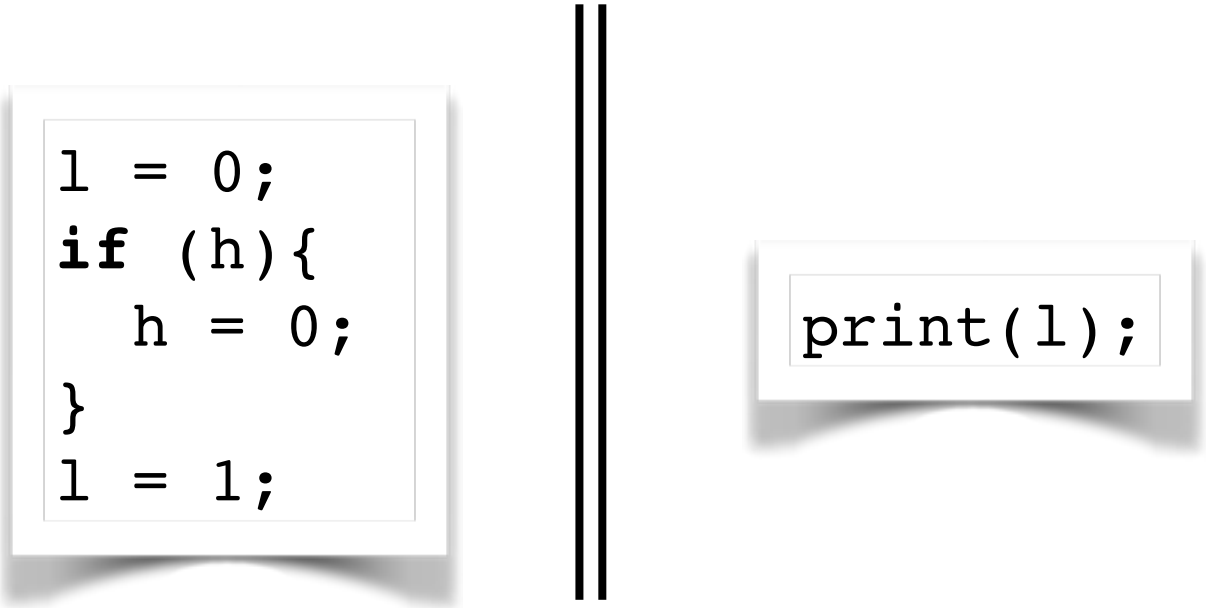

Secure?

Timing-Insensitive Security:

Minimum Requirements

(h = 0)

pc

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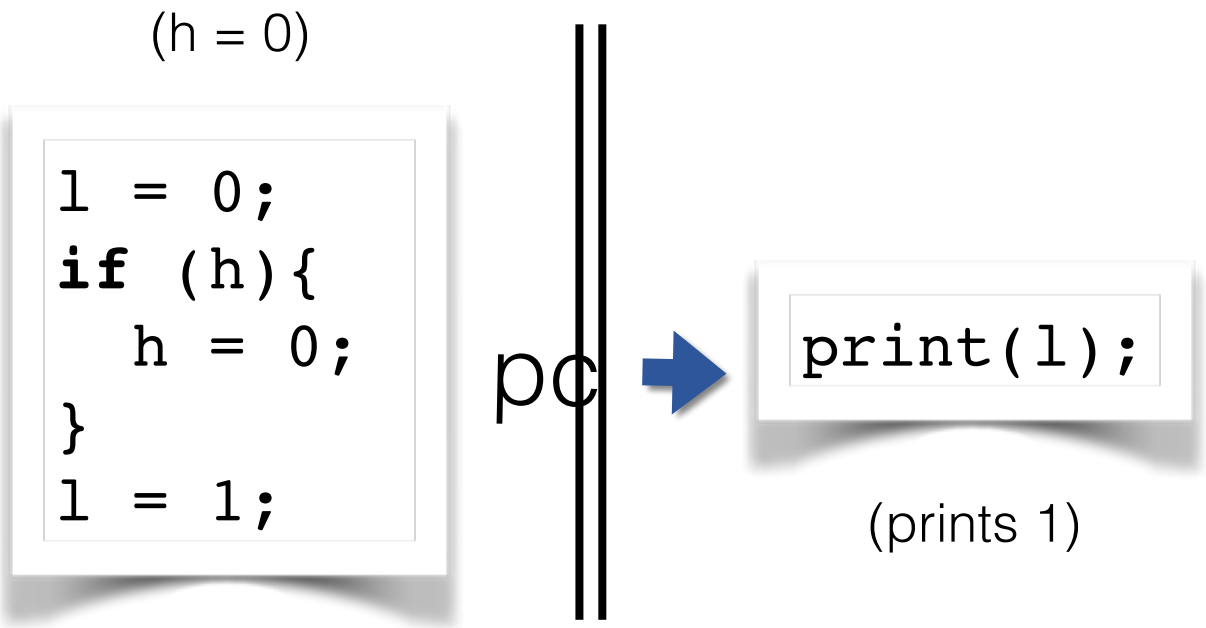

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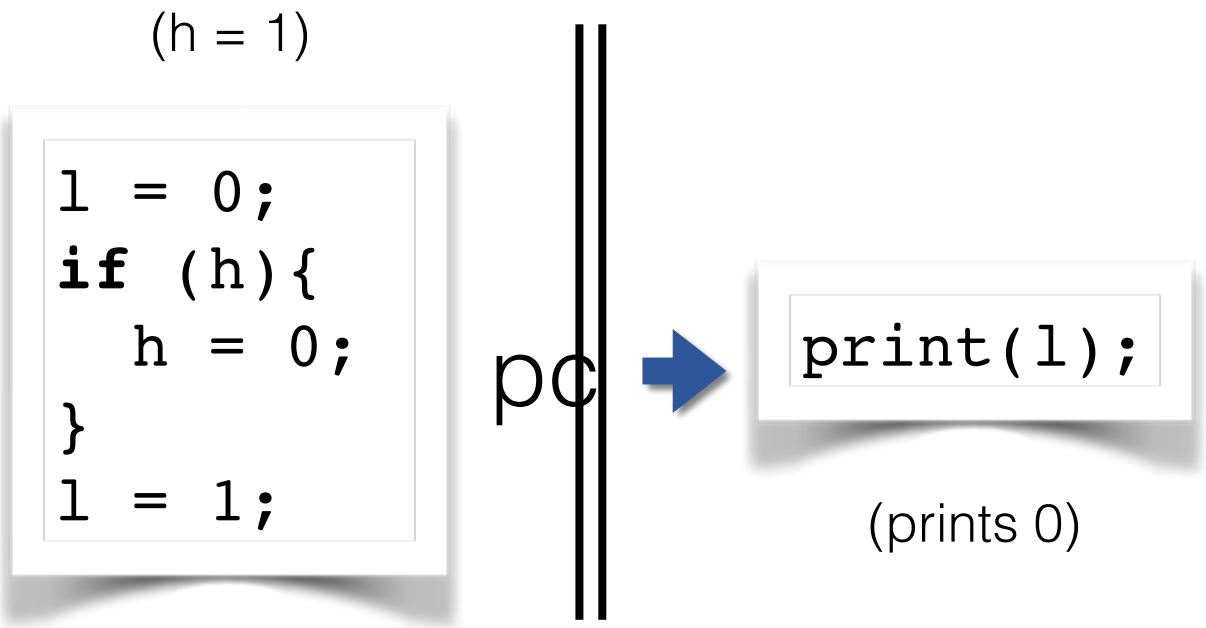
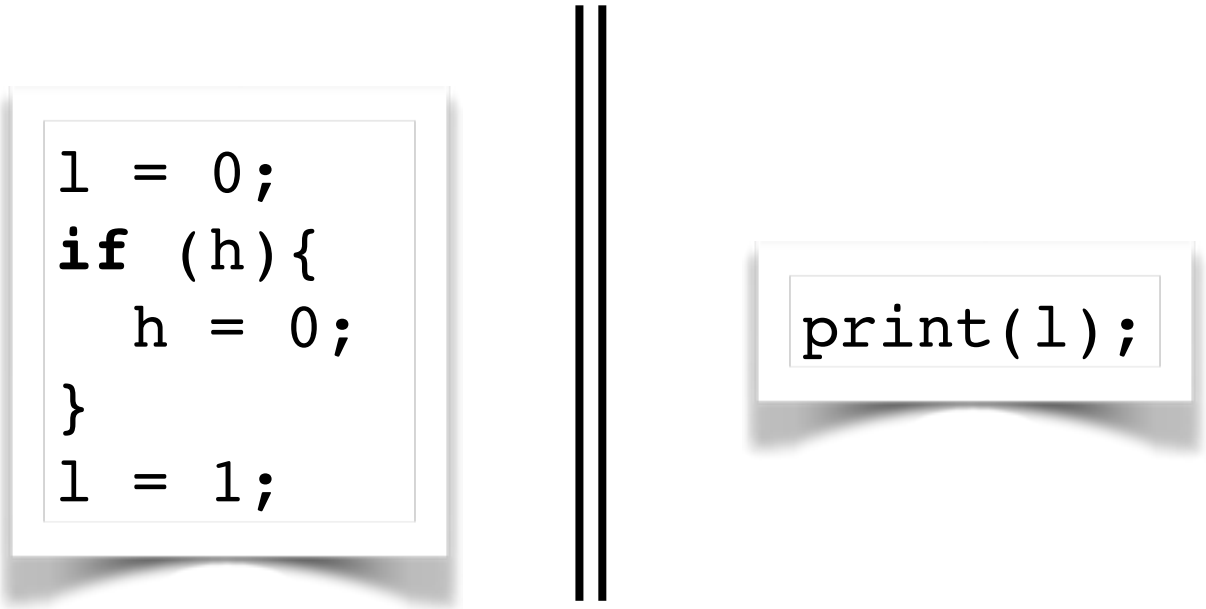


Secure?

Timing-Insensitive Security:

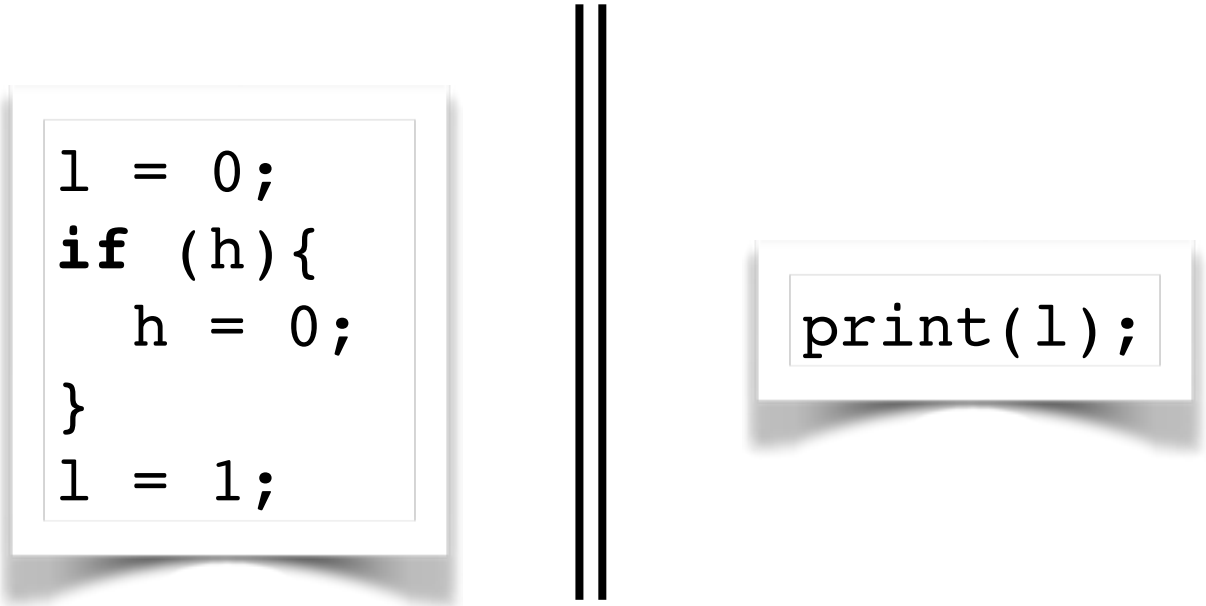
Minimum Requirements



Secure?

Timing-Insensitive Security:

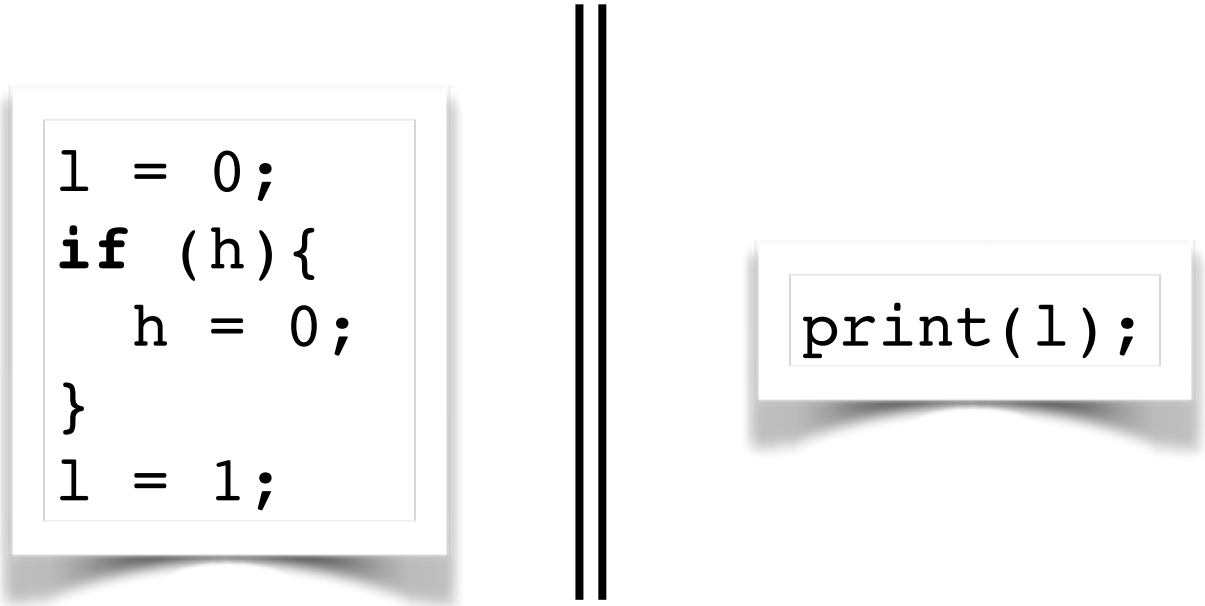
Minimum Requirements



Secure?

Timing-Insensitive Security: **NO**

Minimum Requirements



Secure?

Timing-Insensitive Security: **NO**

Timing-Sensitive Security:

Minimum Requirements

```
l = 0;
if (h){
  h = 0;
}
l = 1;
```

||

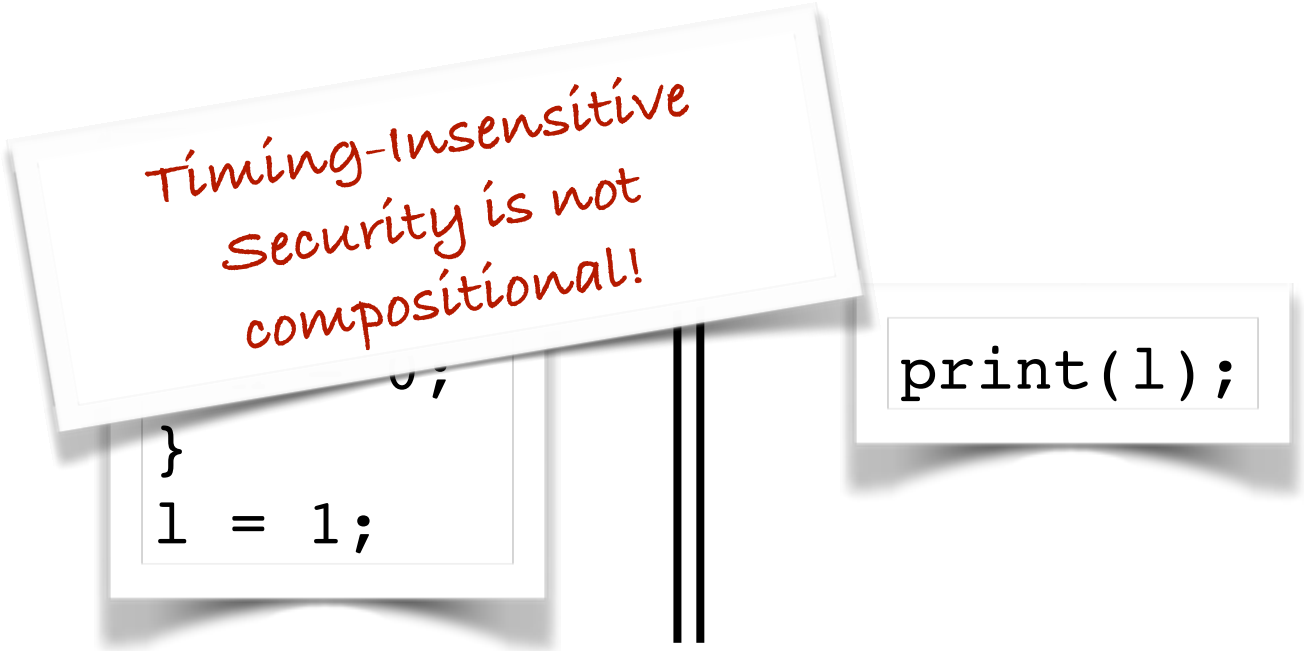
```
print(l);
```

Secure?

Timing-Insensitive Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

Minimum Requirements

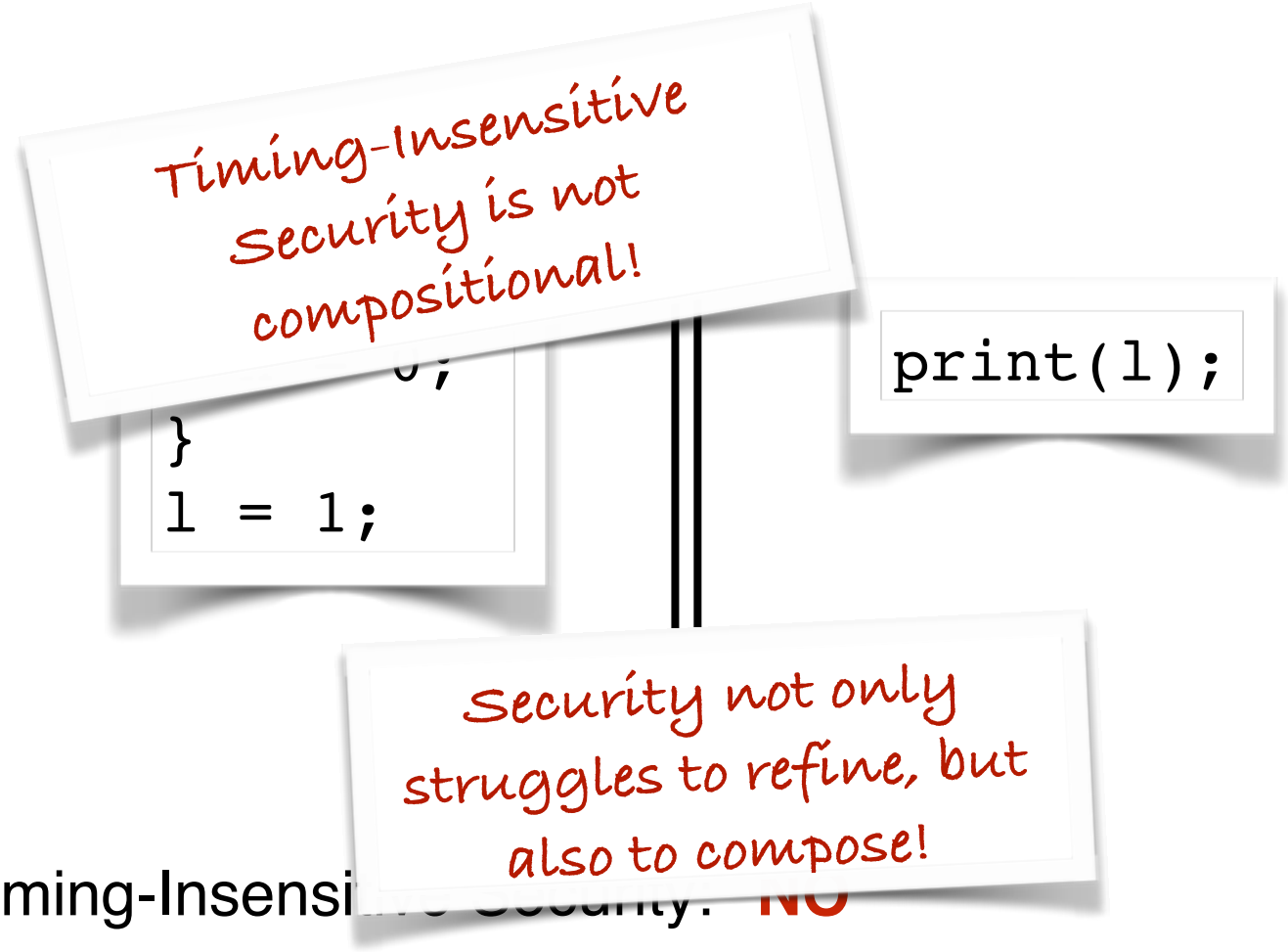


Secure?

Timing-Insensitive Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

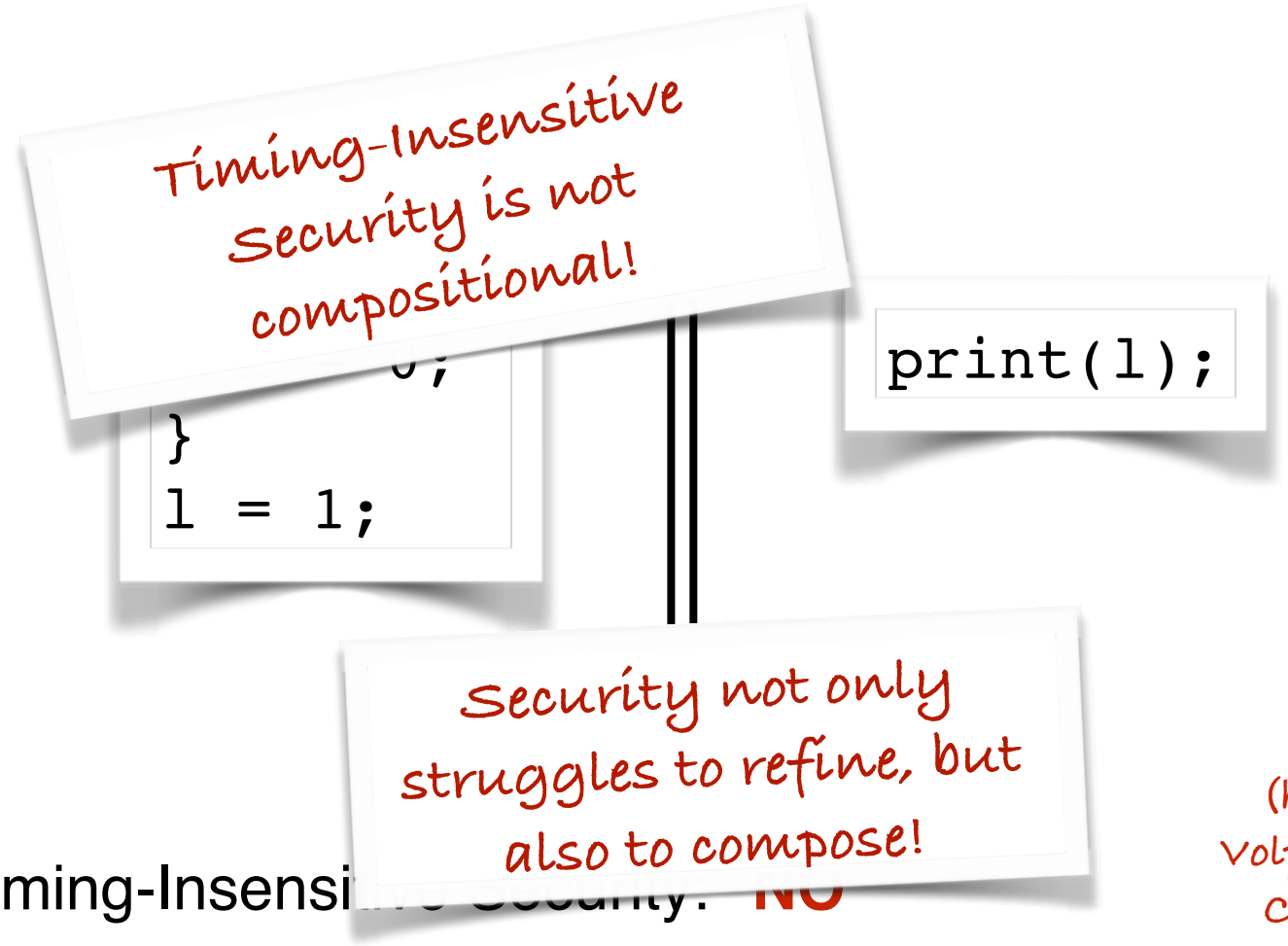
Minimum Requirements



Timing-Insensi… Security: **NO**

Timing-Sensitive Security: **NO** (trivially)

Minimum Requirements



(known since Volpano & Smith, CSFW 1998)

Timing-Insensi… Security: **NO**

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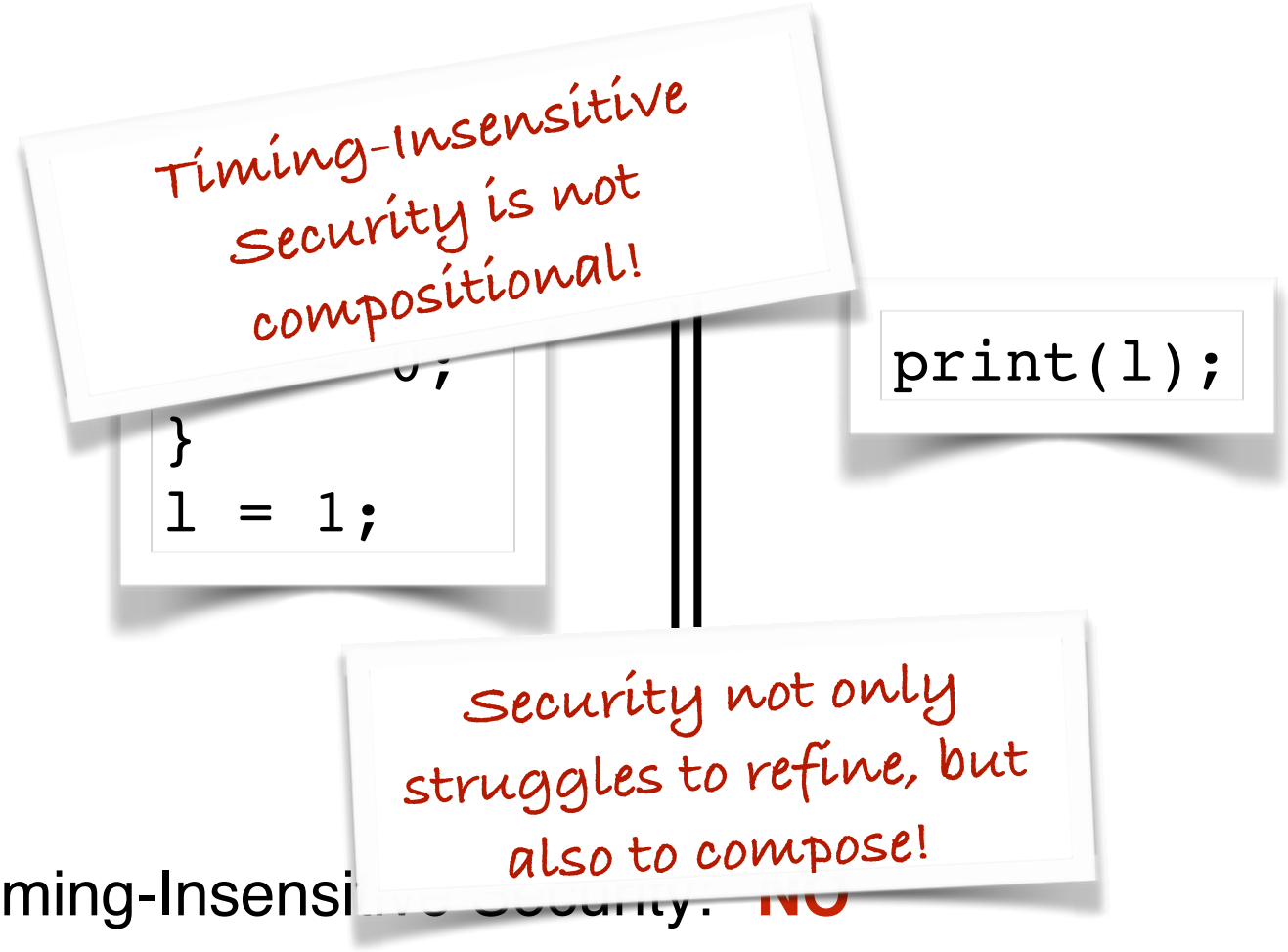
Minimum Requirements



Timing-Insensi… Security: **NO**

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Compositional, Value-Dependent Security

```
/* {dMode,sMode,temp} += AsmNoRW */
/* acquire (dMode == sMode) */
temp := buffer;
if sMode == 0 then
  low-var := temp
else
  high-var := temp
endif;
temp := 0
```

Compositional, Value-Dependent Security

Extension of Mantel, Sands & Sudbrock (CSF 2011)

```
/* {dMode,sMode,temp} += AsmNoRW */
/* acquire (dMode == sMode) */
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```

Compositional, Value-Dependent Security

```
var dMode              // clas: Low
var high_var           // clas: High
var low_var, sMode     // clas: Low
var buffer             // clas: dMode == 0 ? Low : High
```

```
/* {dMode,sMode,temp} += AsmNoRW */
/* acquire (dMode == sMode) */
temp := buffer;
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value-dependent classification

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Compositional, Value-Dependent Security

control variable (must be statically Low)

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var dMode                 // clas: Low
var high_var              // clas: High
var low_var, sMode        // clas: Low
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dynamic, local assumptions about environment, for compositional reasoning

Compositional Reasoning

Compositional Reasoning

Dynamic Modes:

Compositional Reasoning

Dynamic Modes:

```
R :: state rel
```

Compositional Reasoning

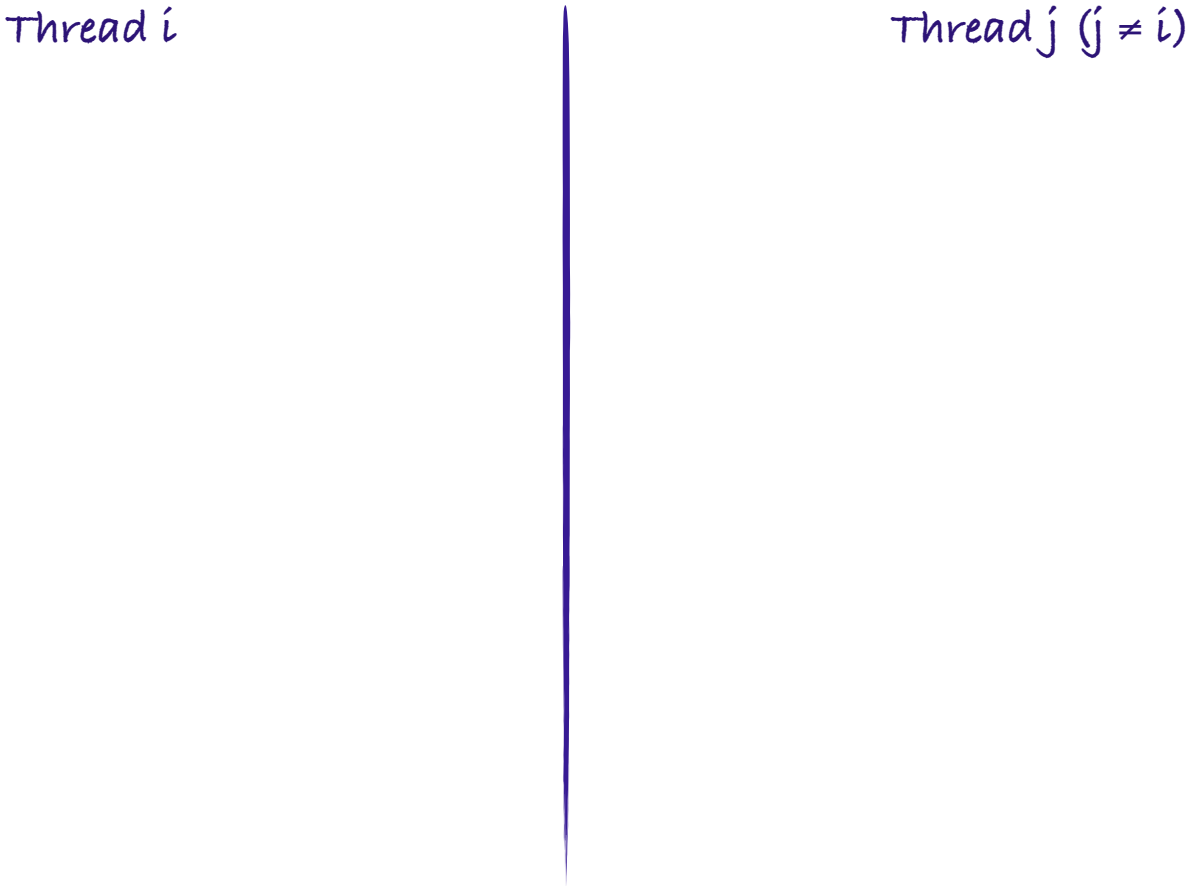
Dynamic Modes: `R :: state rel`

`NoReadOrWrite x`

Compositional Reasoning

Dynamic Modes: `R :: state rel`

`NoReadOrWrite x`



Compositional Reasoning

Dynamic Modes: `R :: state rel`

`NoReadOrWrite x`

Thread i

Thread j ($j \neq i$)

```
// assume: mode
```

Compositional Reasoning

Dynamic Modes: `R :: state rel`

`NoReadOrWrite x`

Thread i

```
// assume: mode

...
```

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Compositional Reasoning

Dynamic Modes: `R :: state rel`

`NoReadOrWrite x`

Thread i

```
// assume: mode

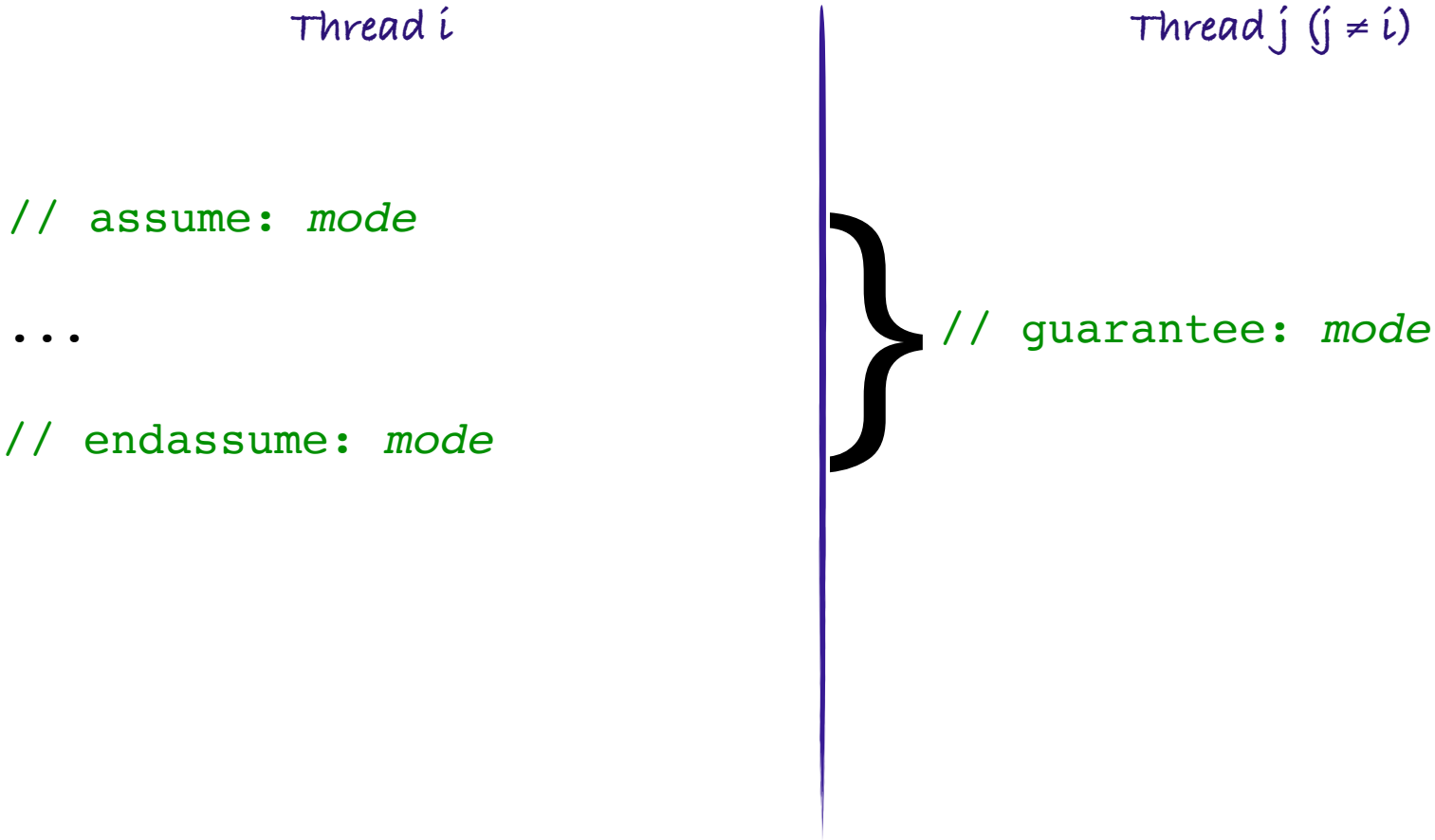
...

// endassume: mode
```

Thread j (j ≠ i)

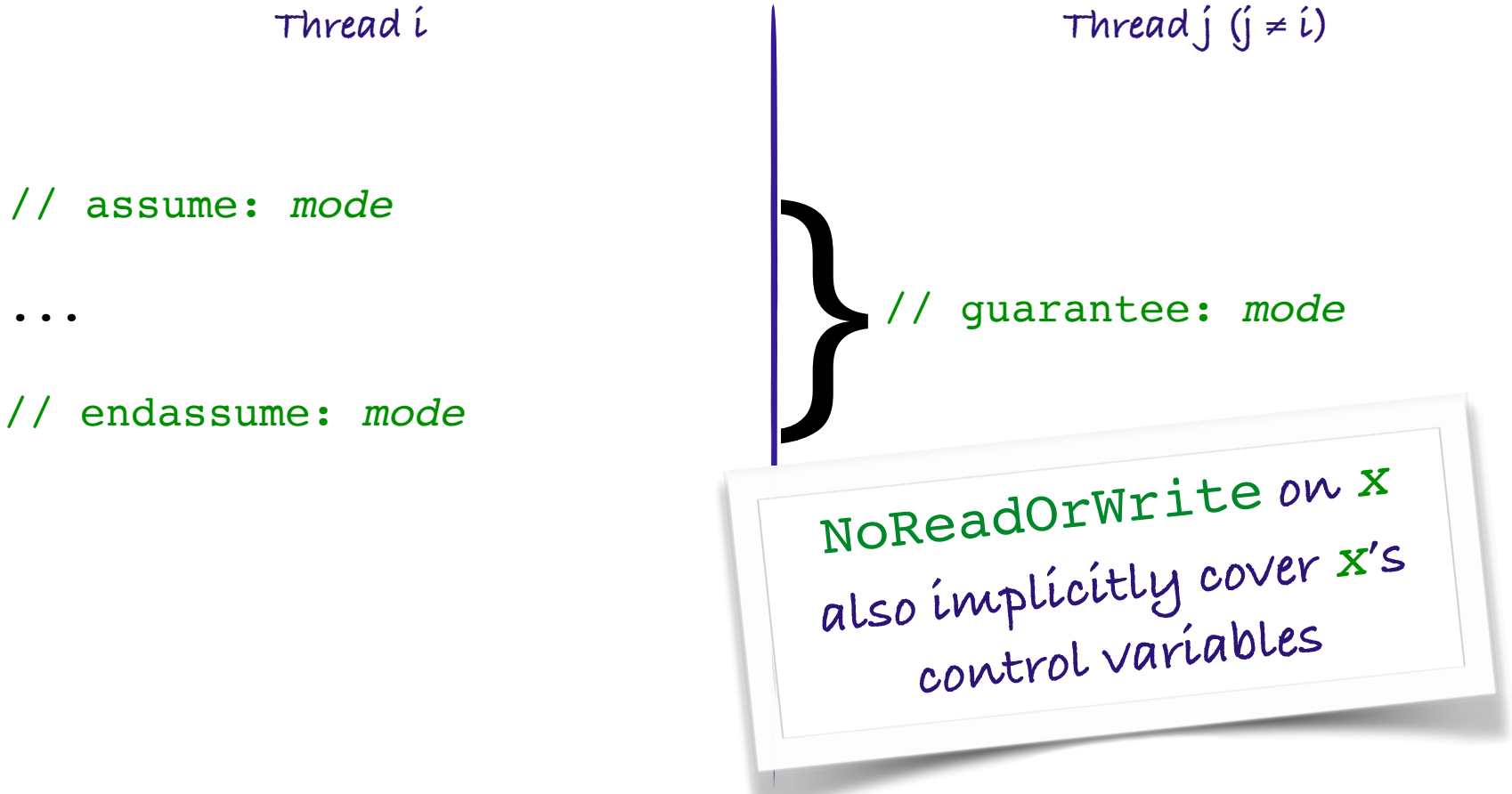
Compositional Reasoning

Dynamic Modes: `R :: state rel` `NoReadOrWrite x`



Compositional Reasoning

Dynamic Modes: `R :: state rel` `NoReadOrWrite x`



Compositional Reasoning

Dynamic Modes: `R :: state rel`

`NoReadOrWrite x`

Thread i

```
// assume: mode
...
// endassume: mode
```

Thread j (j ≠ i)

```
// guarantee: mode
```

If you `GuarNoReadOrWrite x` then your `assume R` can't mention `x`

`NoReadOrWrite` on `x` also implicitly cover `x`'s control variables

Semantics

Semantics

Local Configurations: (c, mds, mem)

Semantics

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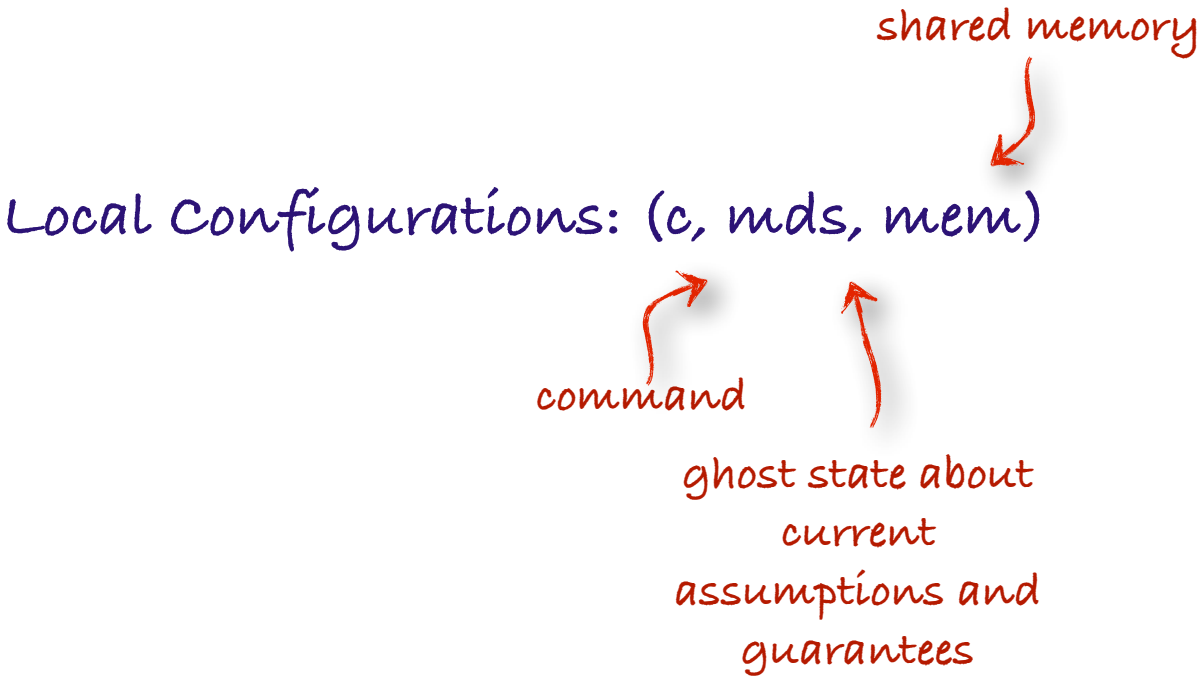
Semantics

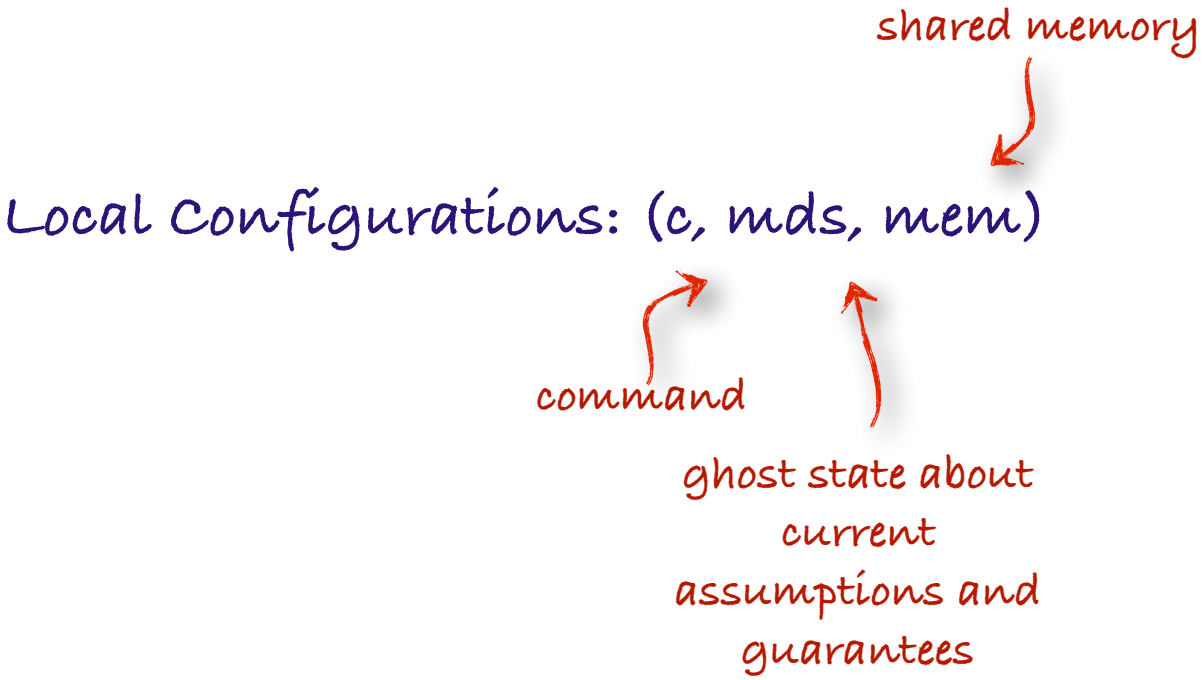
Local Configurations: (c, mds, mem)

ghost state about current assumptions and guarantees

Semantics


shared memory
Local Configurations: (c, mds, mem)
command
ghost state about current assumptions and guarantees

Semantics



Global Configurations: ((c, mds) list, mem)

System Model

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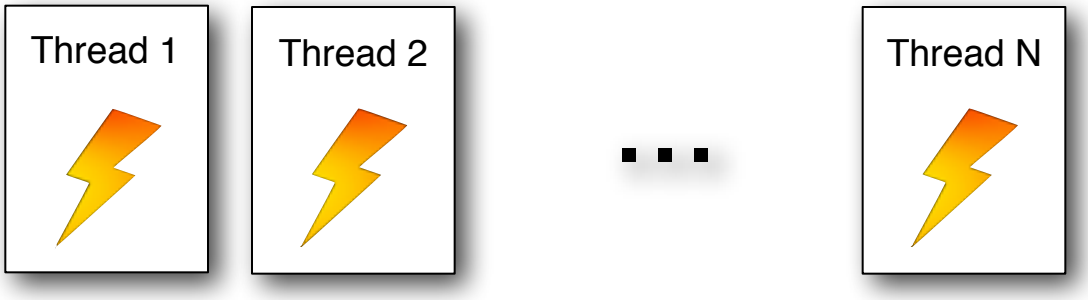

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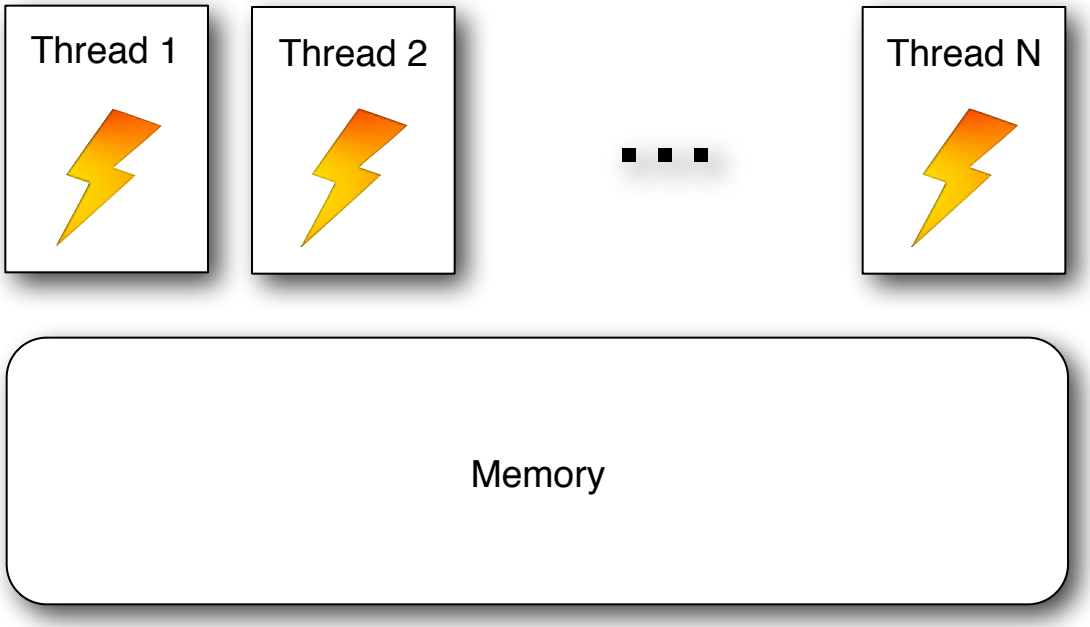

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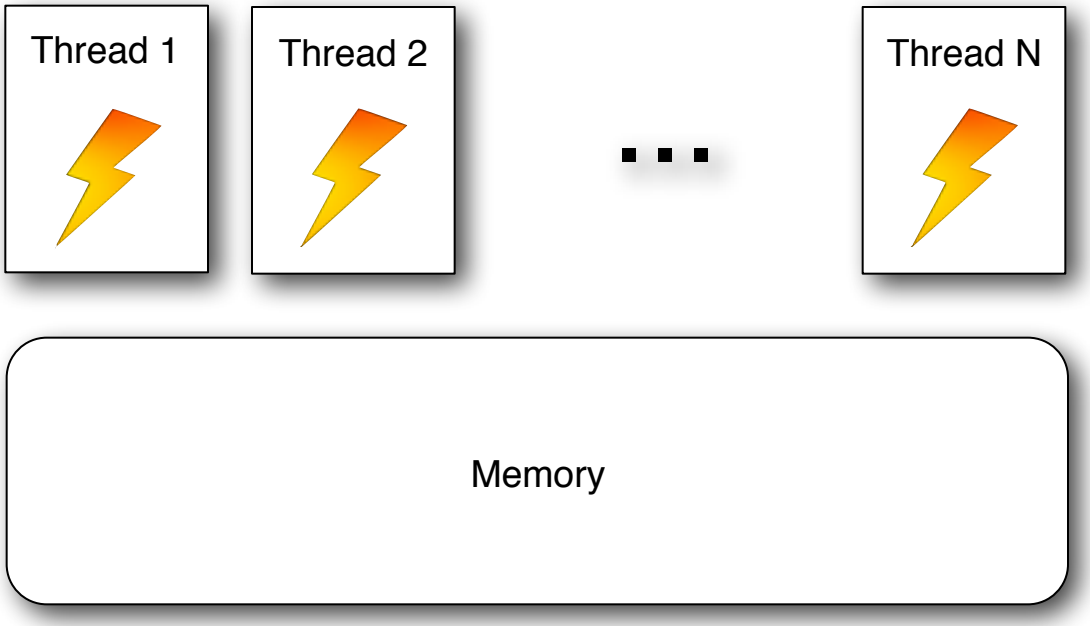
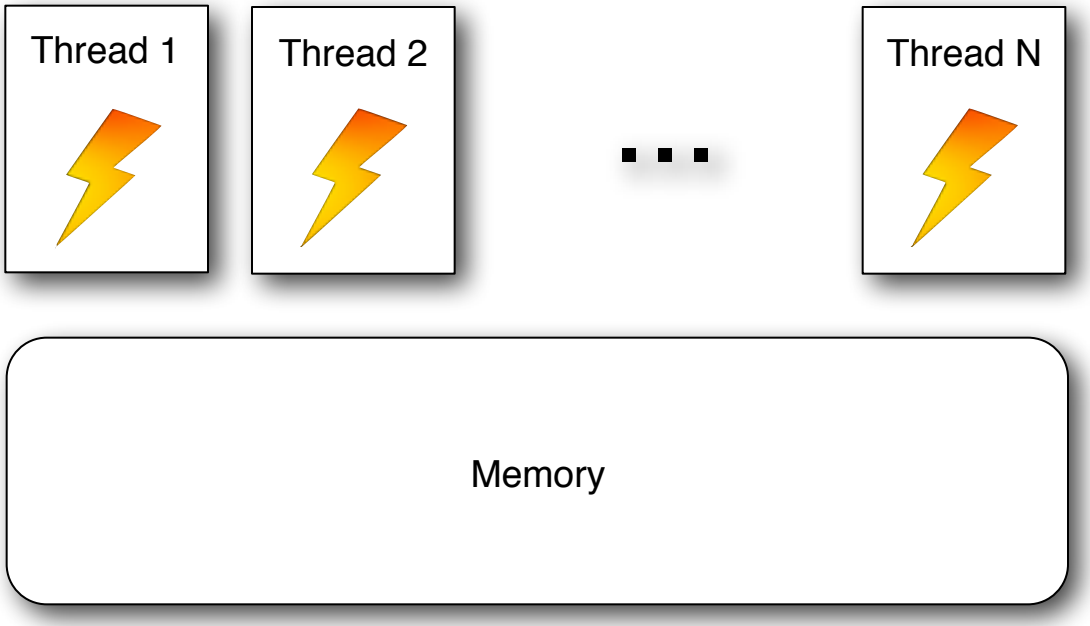


Arbitrary, Static Schedule:

System Model



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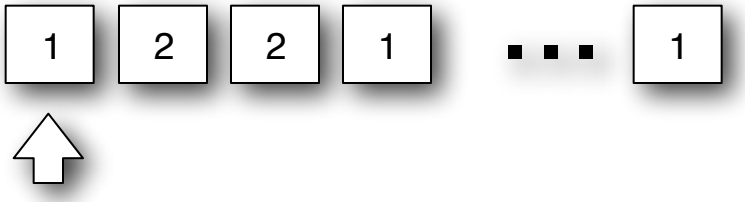
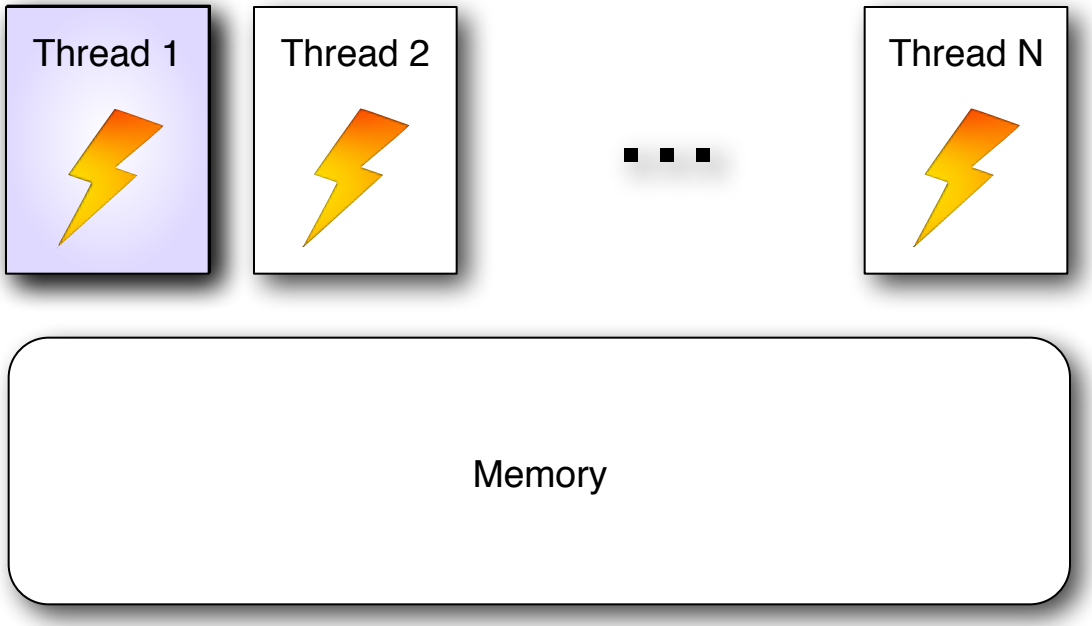
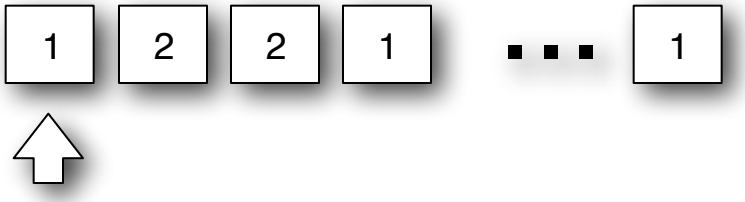


System Model



Arbitrary, Static Schedule:



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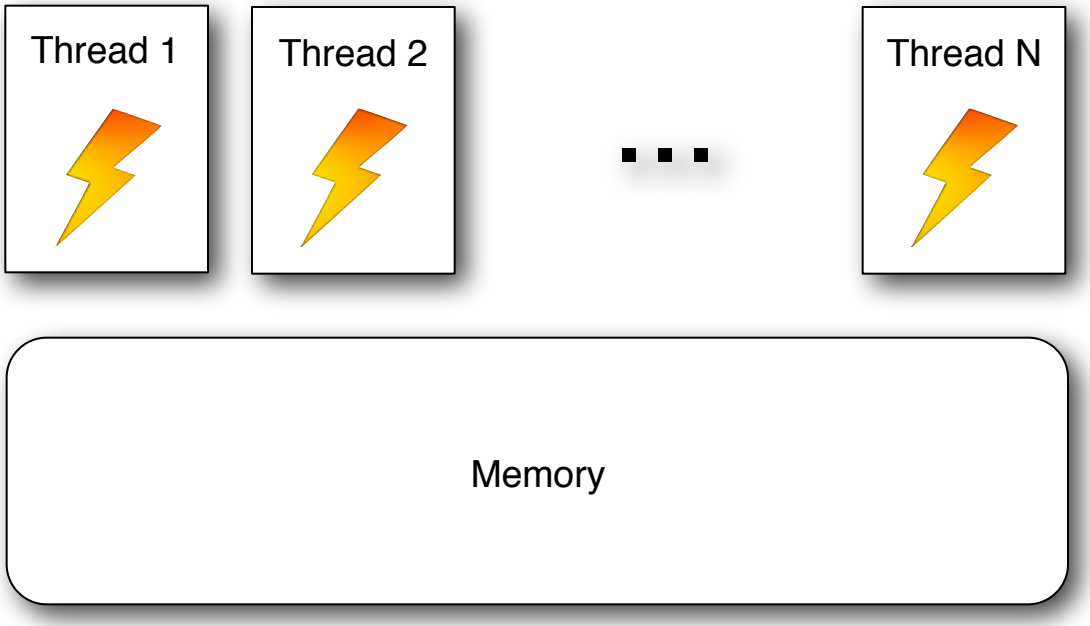

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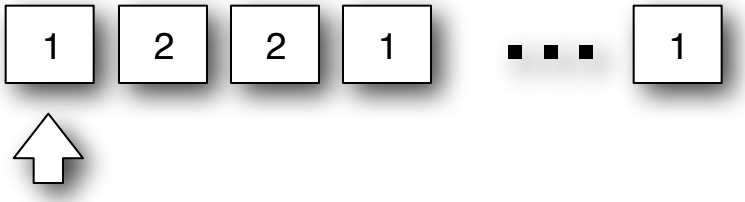

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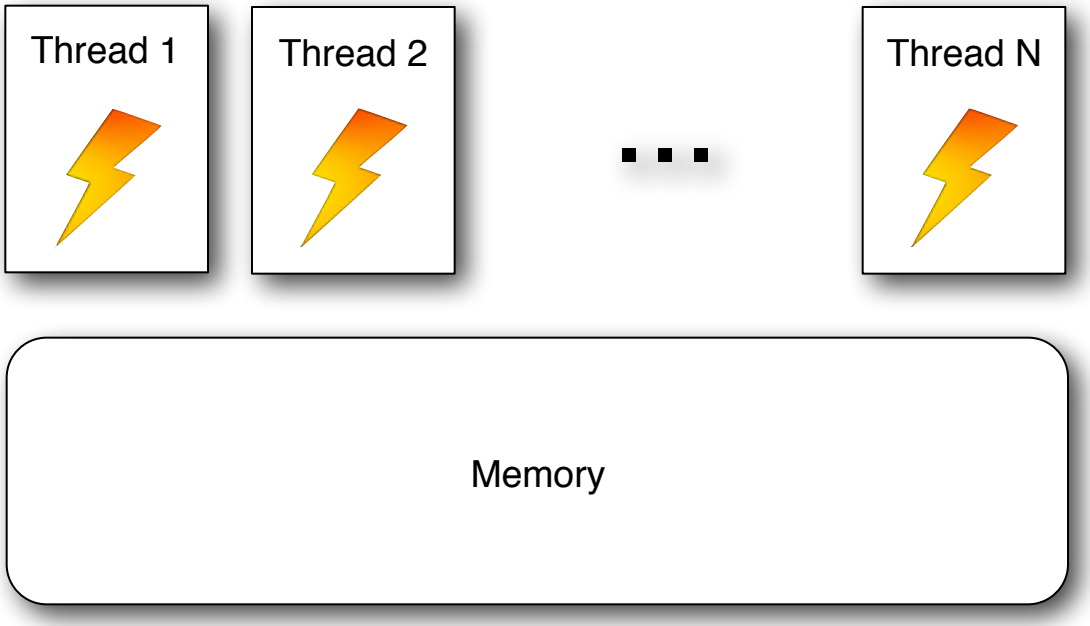

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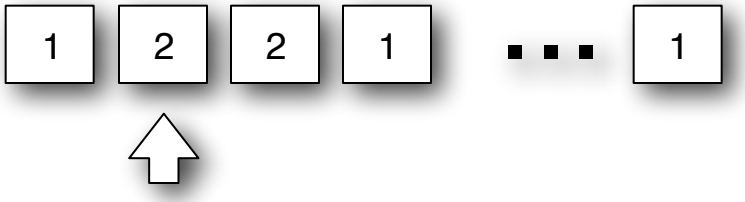

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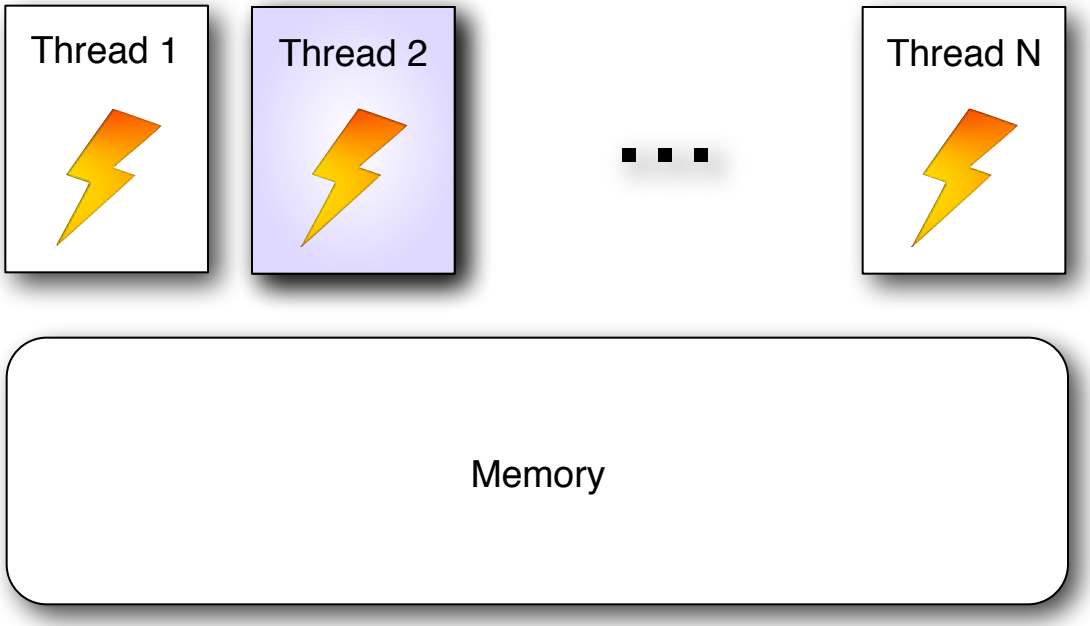

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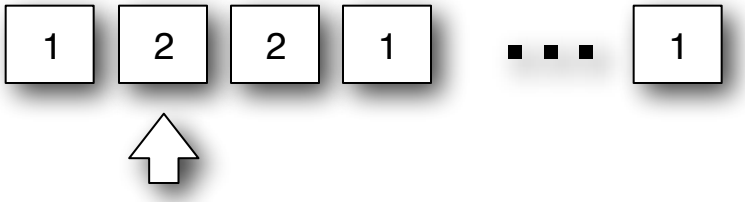

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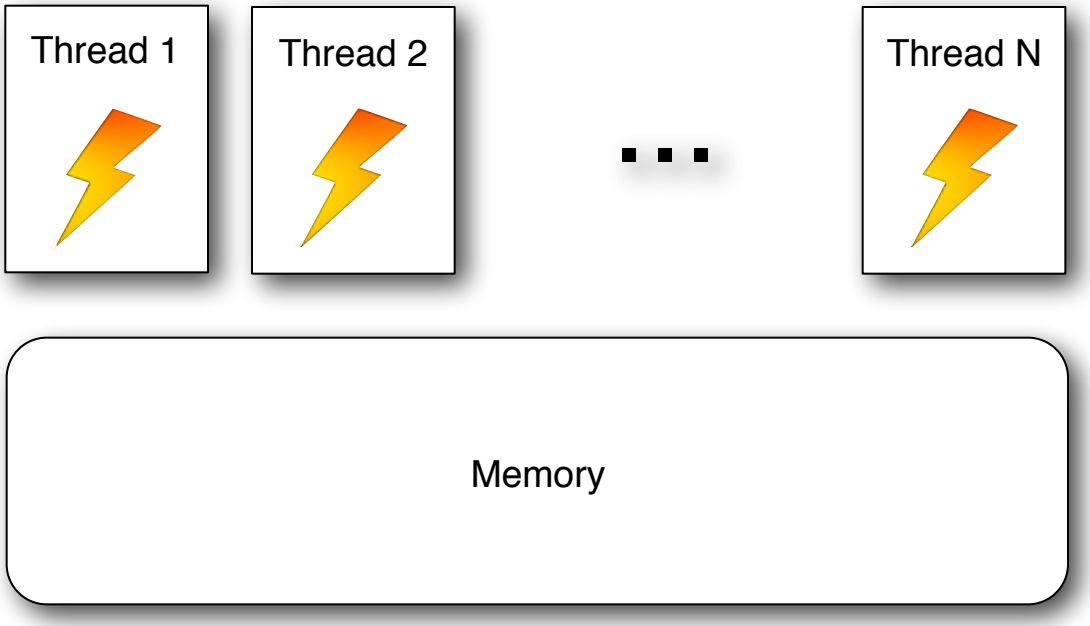

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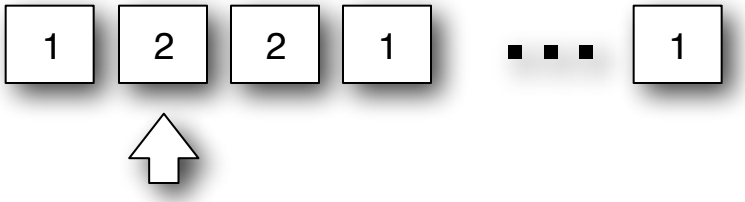

Global Security

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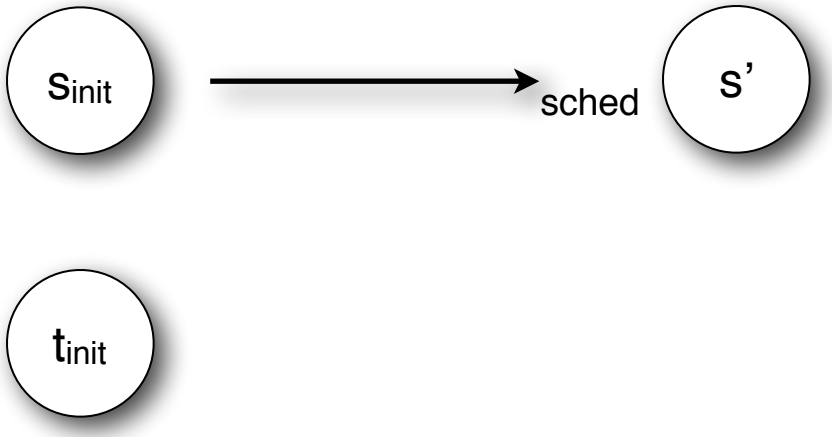

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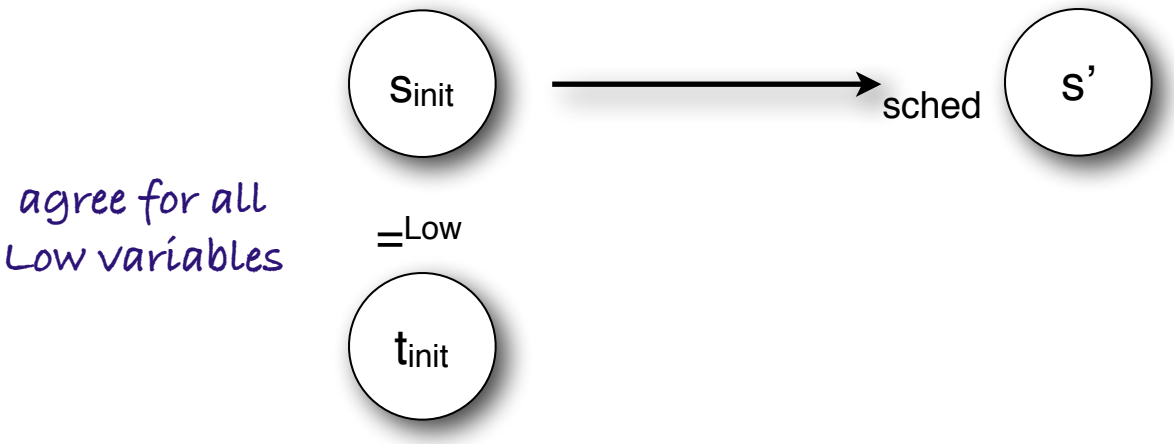

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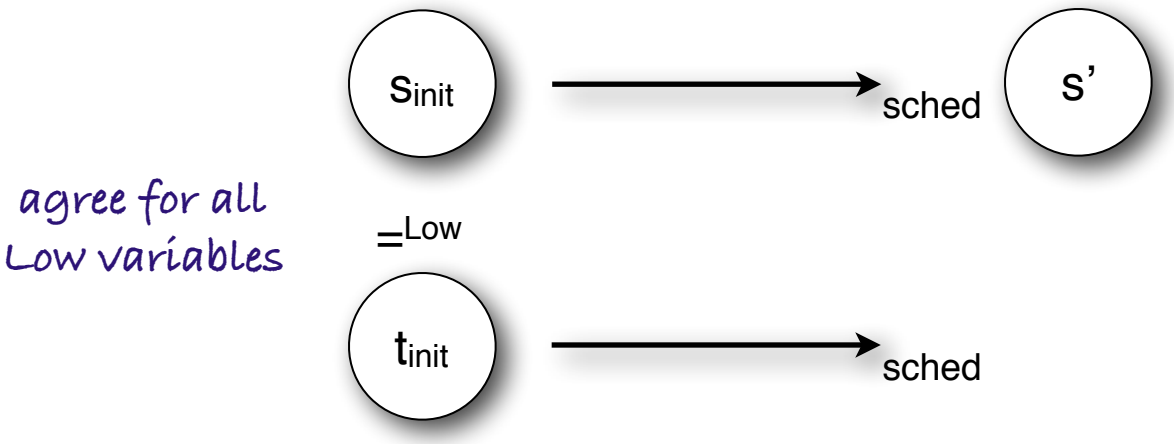
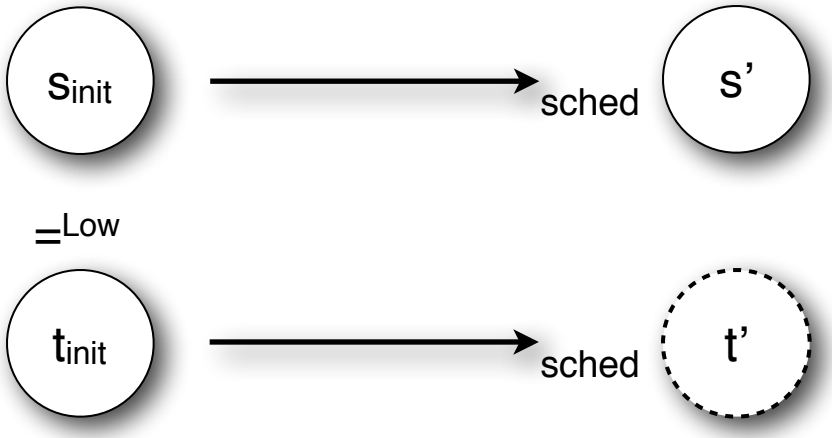


Global Security

agree for all Low variables



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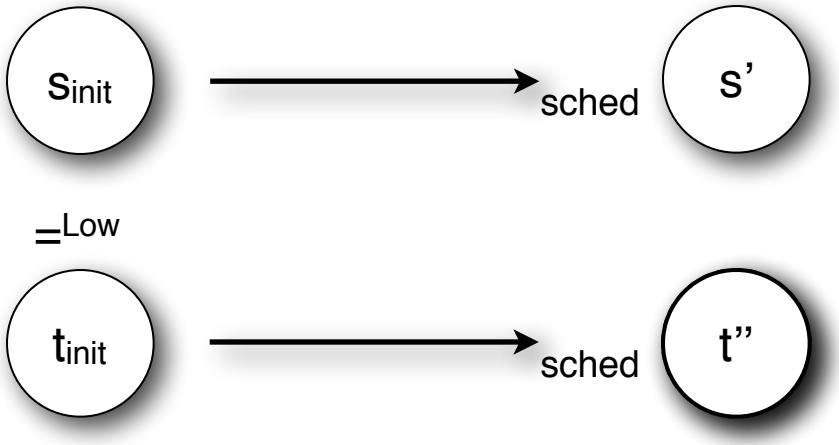

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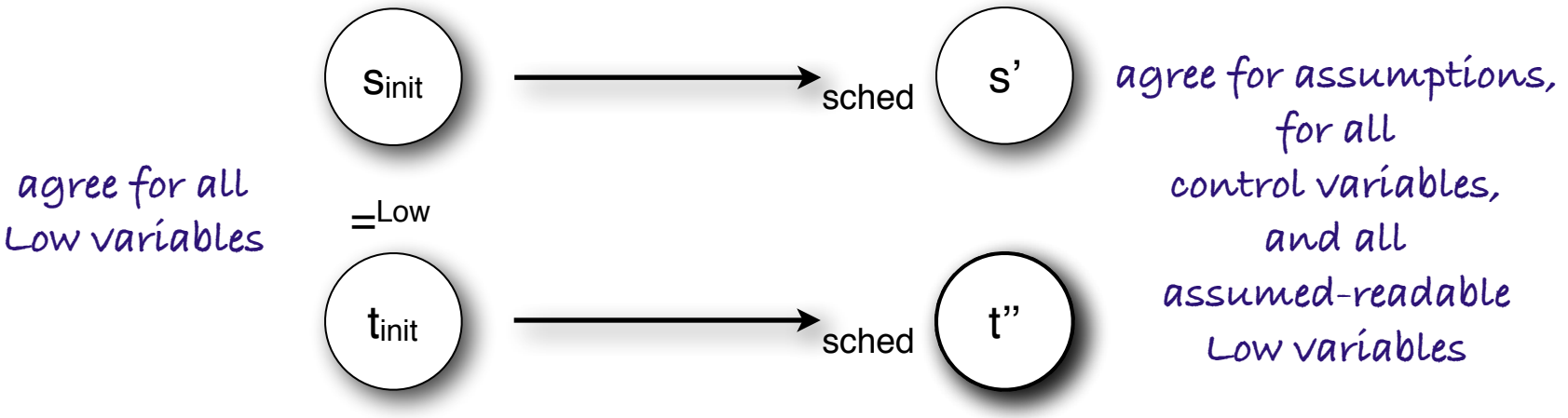

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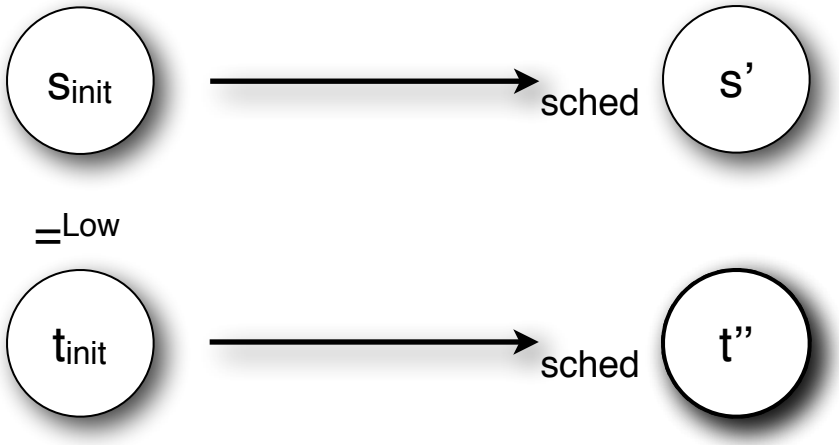

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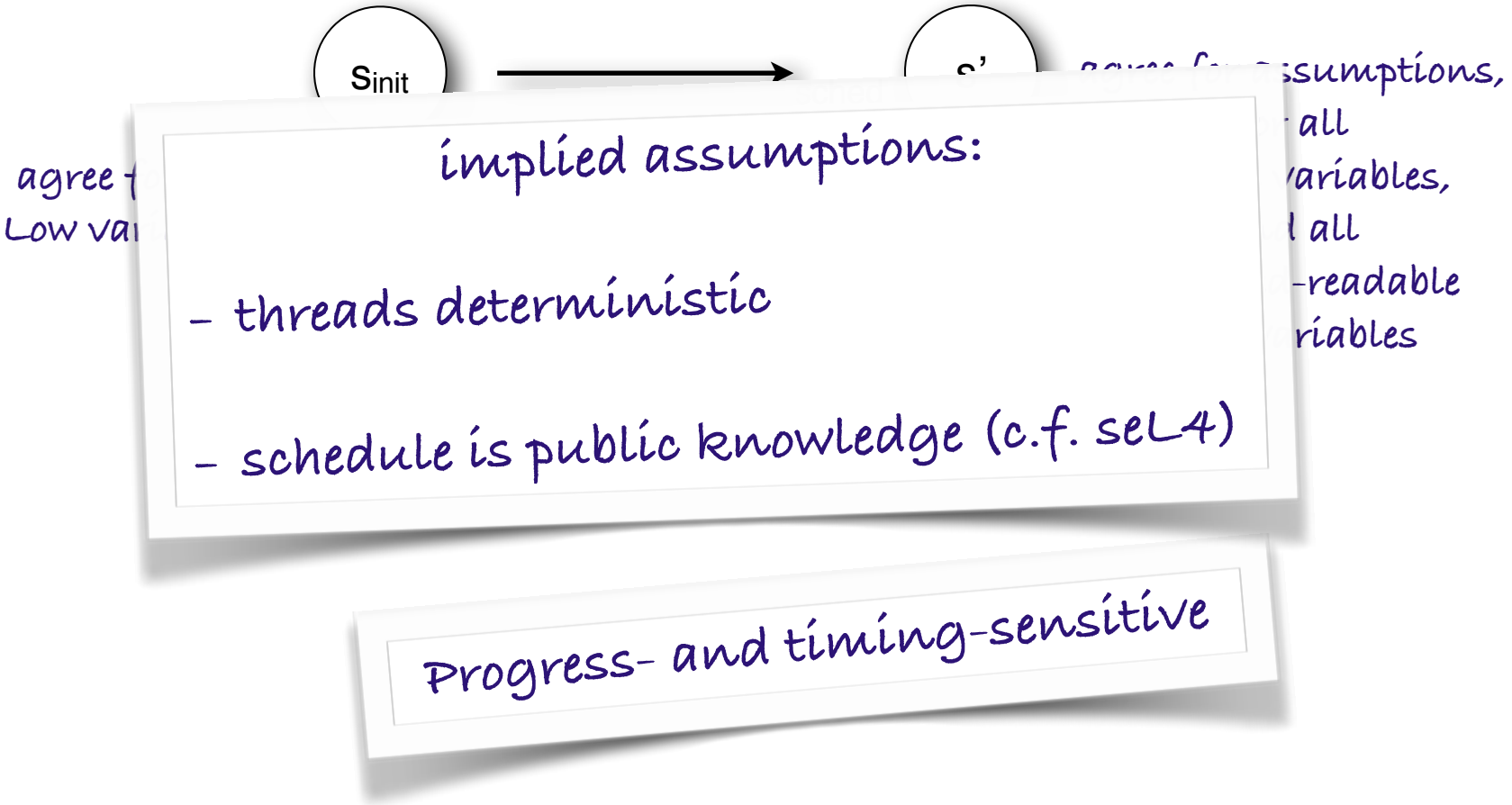
Progress- and timing-sensitive

Global Security



Low Equivalence

Noninterference is essentially preservation of Low-equivalence between all pairs of executions.

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$$mem_1 =_{mds}^{l} mem_2 \equiv$$
$$\forall x.\ x \in \mathcal{C} \vee \mathcal{L}_{mem_1}\ x = \mathsf{Low} \wedge x \notin mds\ \mathbf{AsmNoRW} \longrightarrow$$
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Two states are low equivalent when they agree on:

- All control variables (necessarily all Low)
- All currently-Low variables that might be read across a component boundary

Non-Readable Variables

Our security definition (and toy program language semantics, **with atomic expression evaluation**) would say this program is secure:

```
// {x,y,z} += AsmNoRW
if (h) {
  x := y + z;
  h := 0
} else {
  x := y;
  skip
}
x := 0;
y := 0;
z := 0;
// {x,y,z} -= AsmNoRW
```

Local Security: Intuition

Local Security: Intuition

Thread i

Local Security: Intuition

We need to prove:

Thread i

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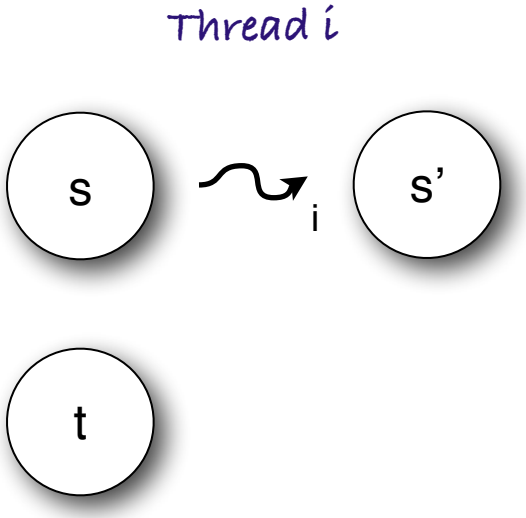

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agree for assumptions,
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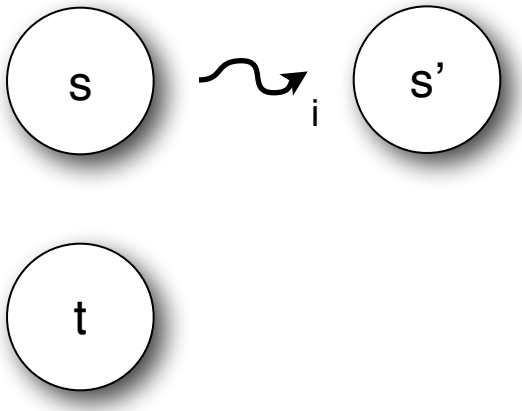

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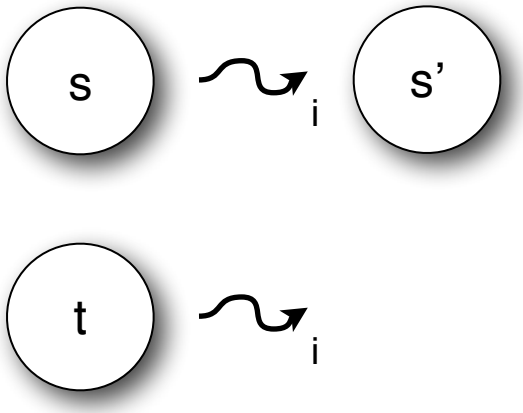

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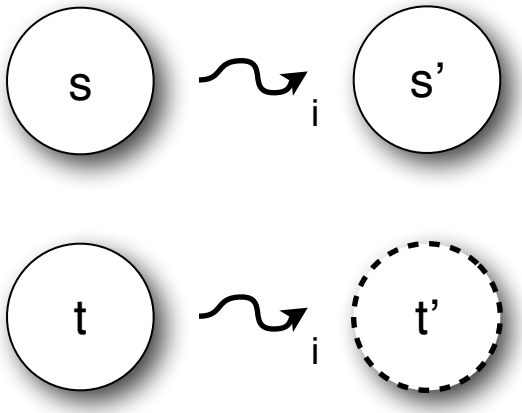

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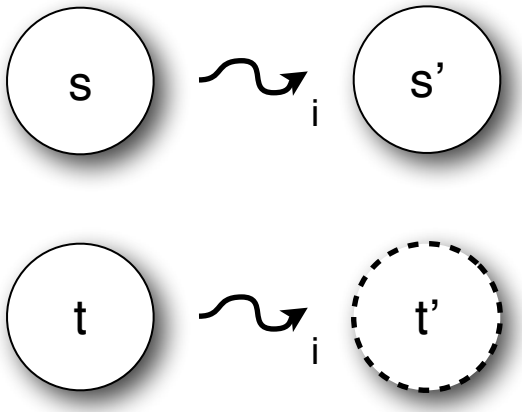

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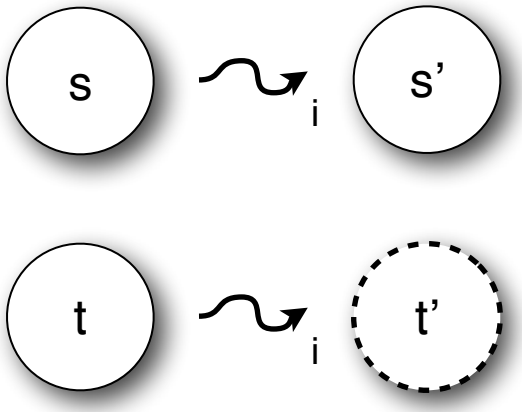

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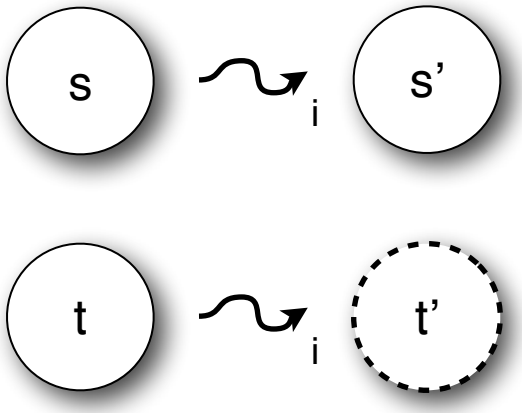

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Proof technique:
(Rely-Guarantee
(bi)simulation

Local Security

Local Security

Find a relation $\mathcal{R}_i$ such that:

Local Security

Find a relation $\mathcal{R}_i$ such that:

Thread i

Local Security

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Thread i

if

Local Security

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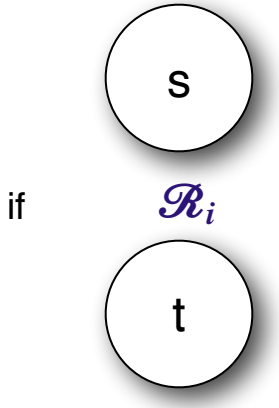

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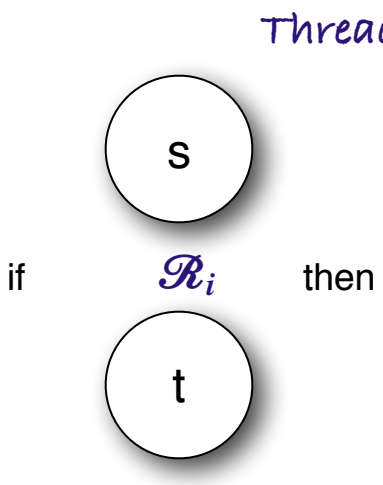

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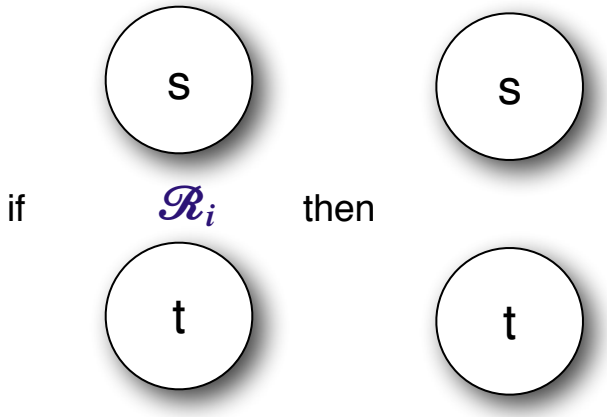

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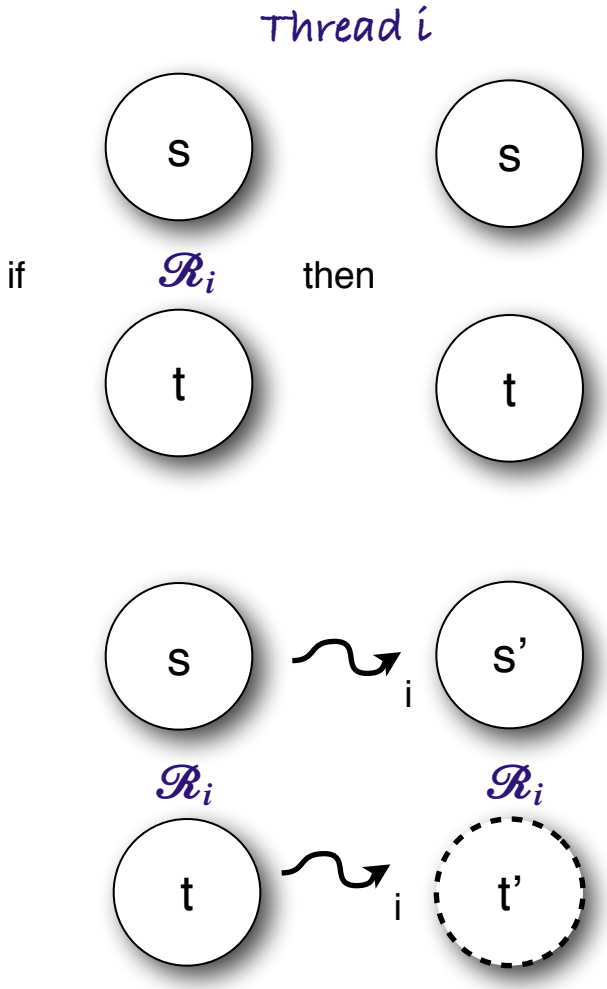

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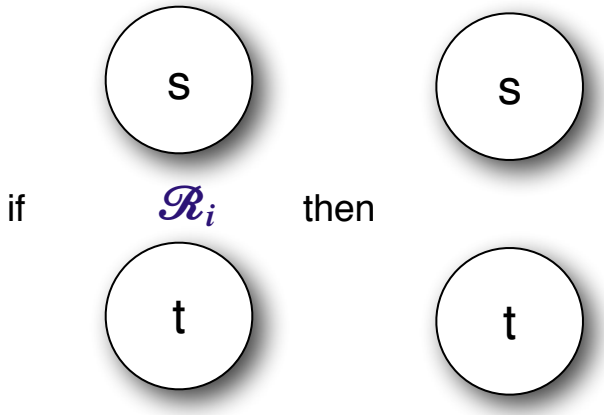

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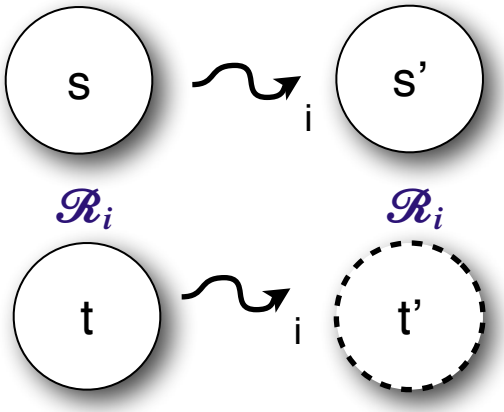
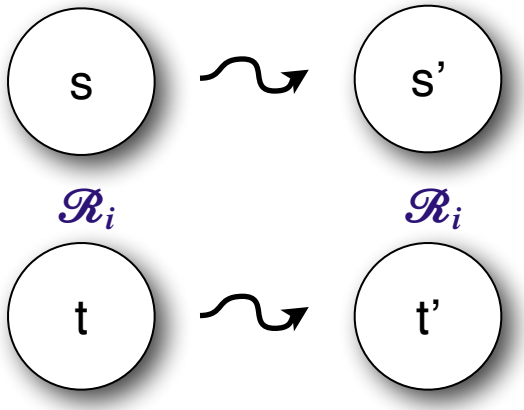
Environment





Local Security

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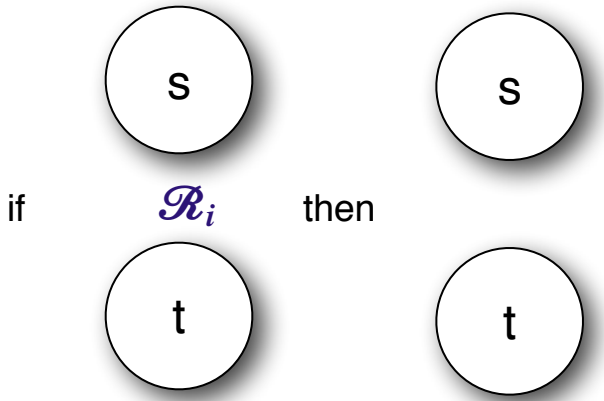

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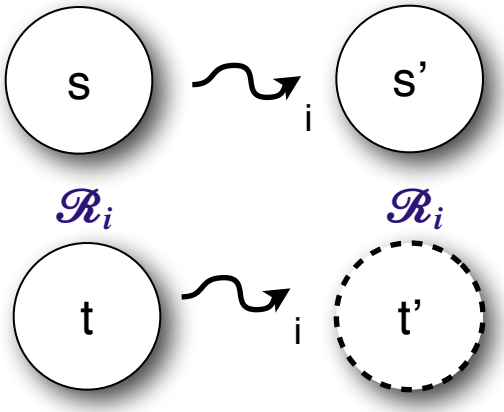
security-preserving
steps that
respect i's current
assumptions



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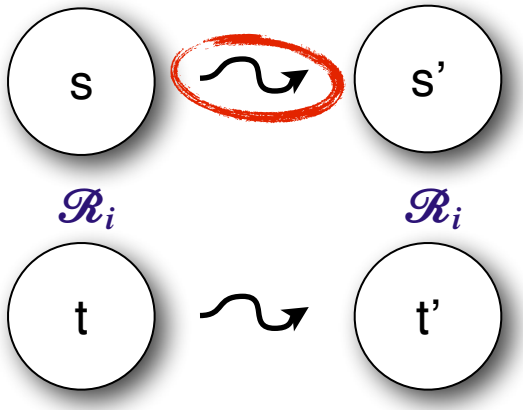
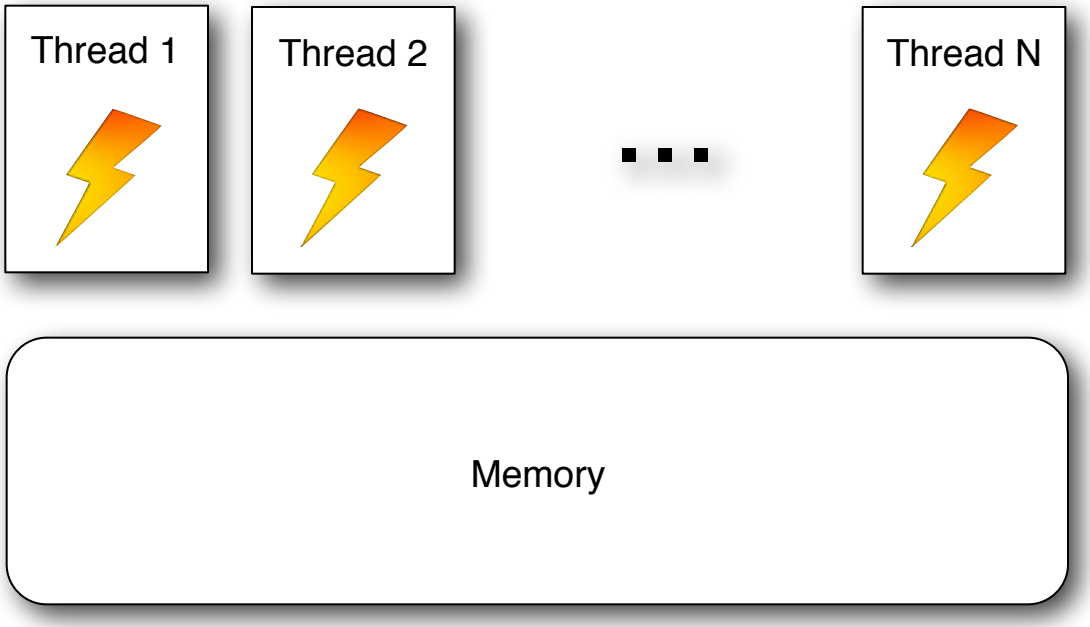


Compositionality Theorem



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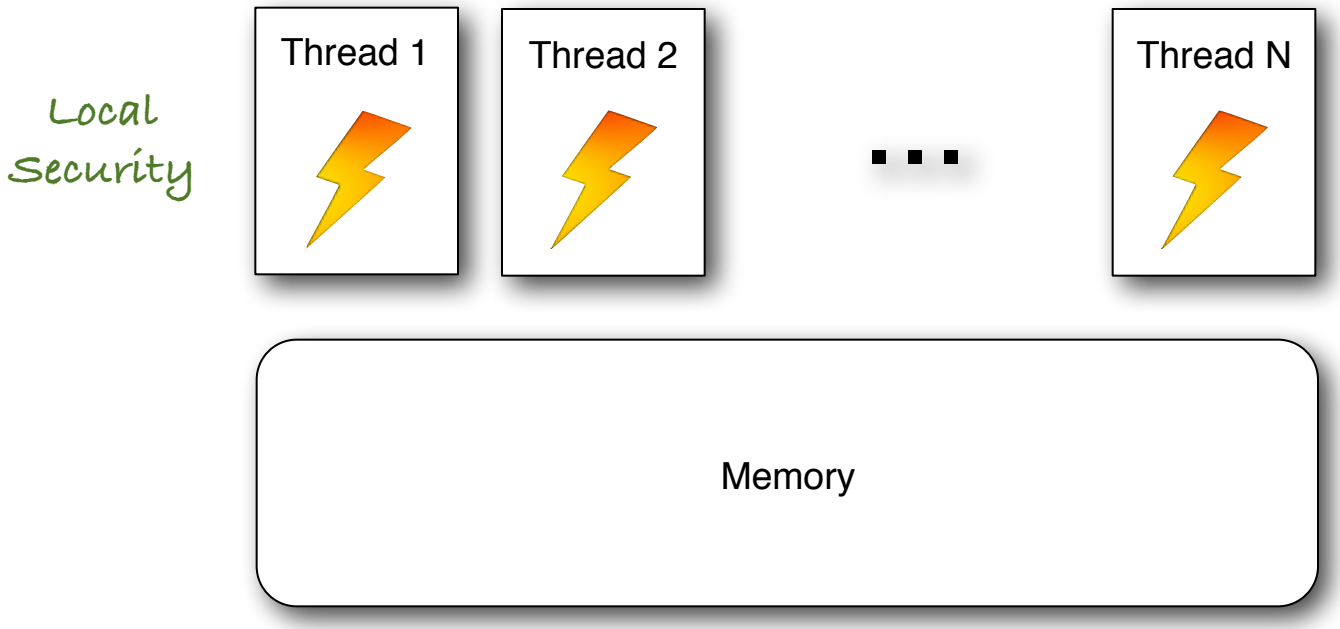

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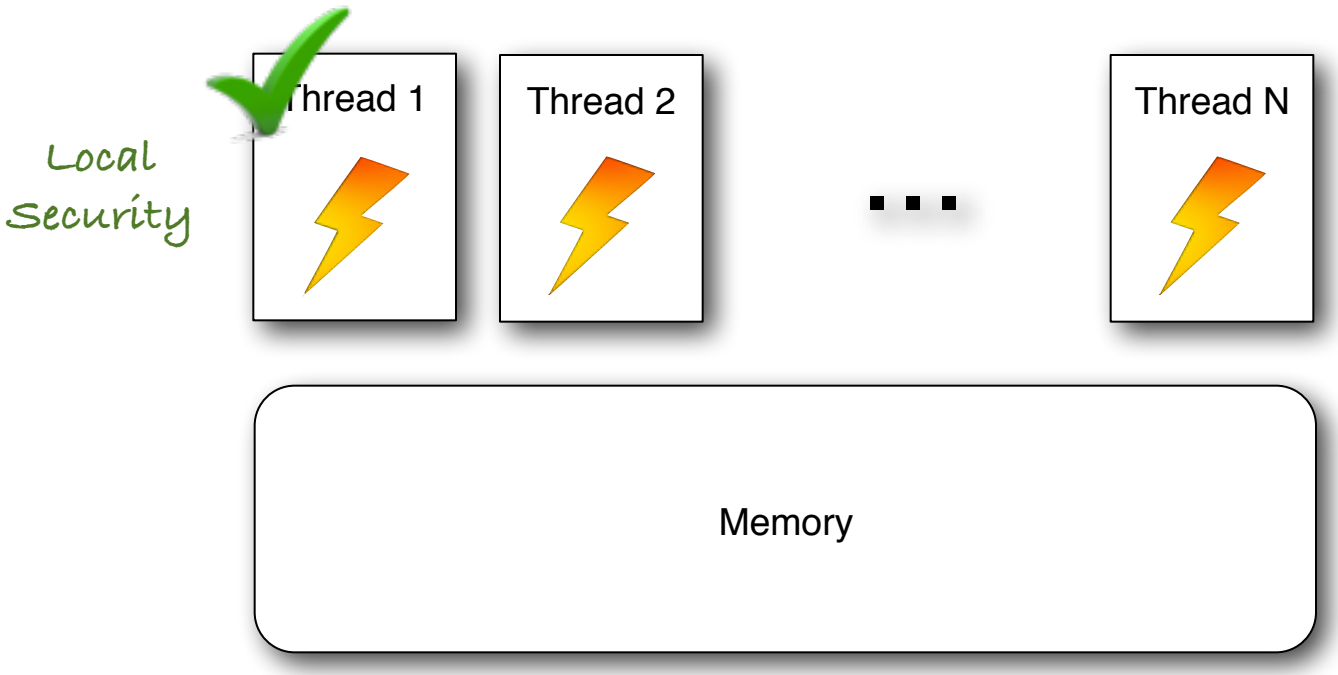

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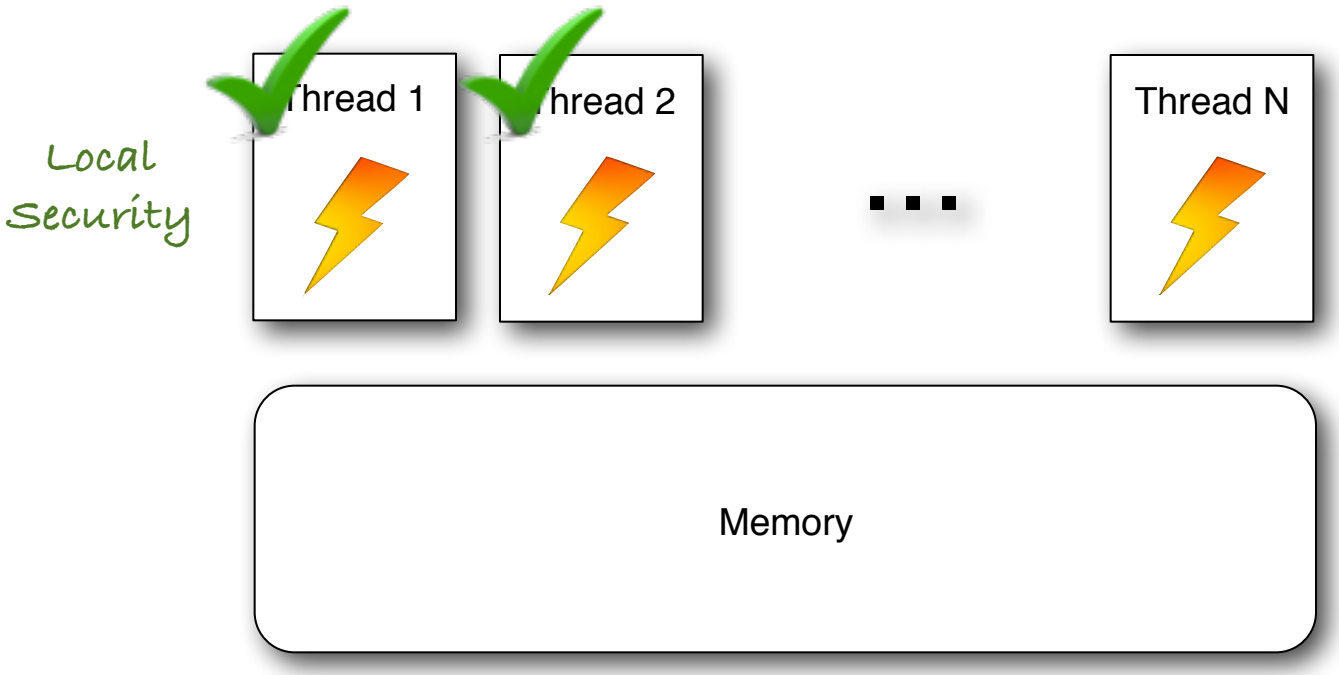

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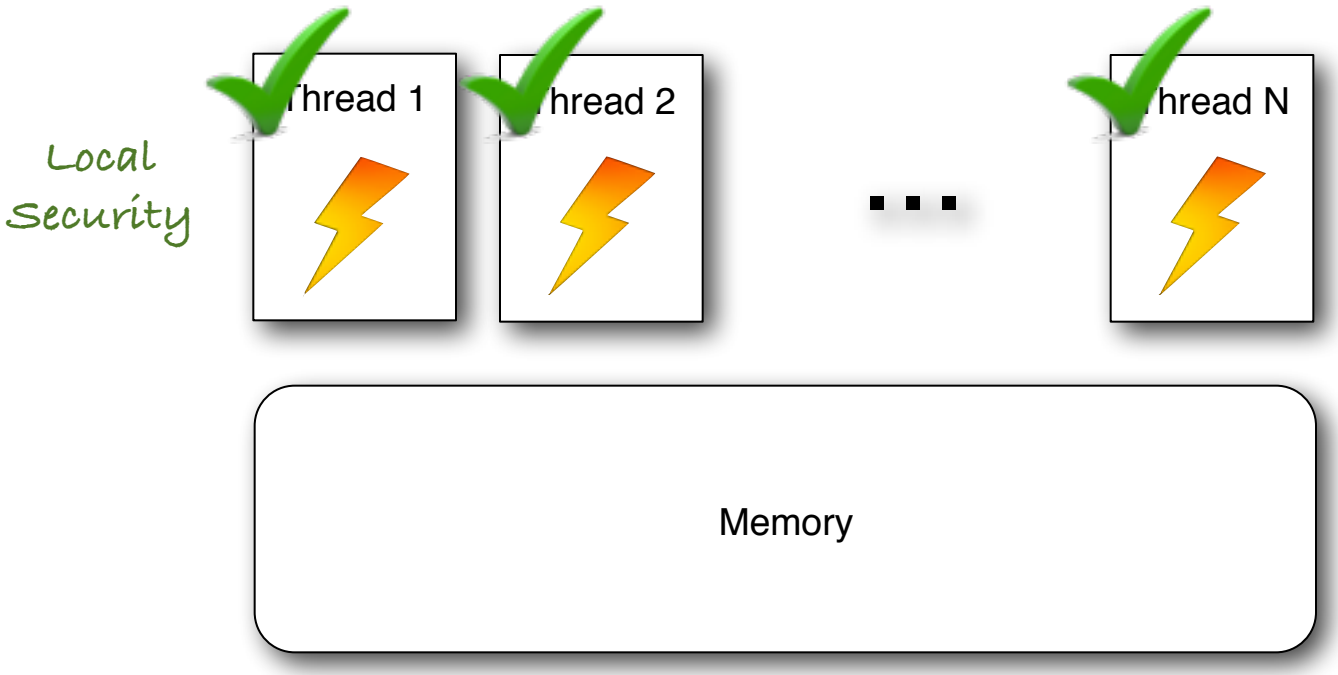

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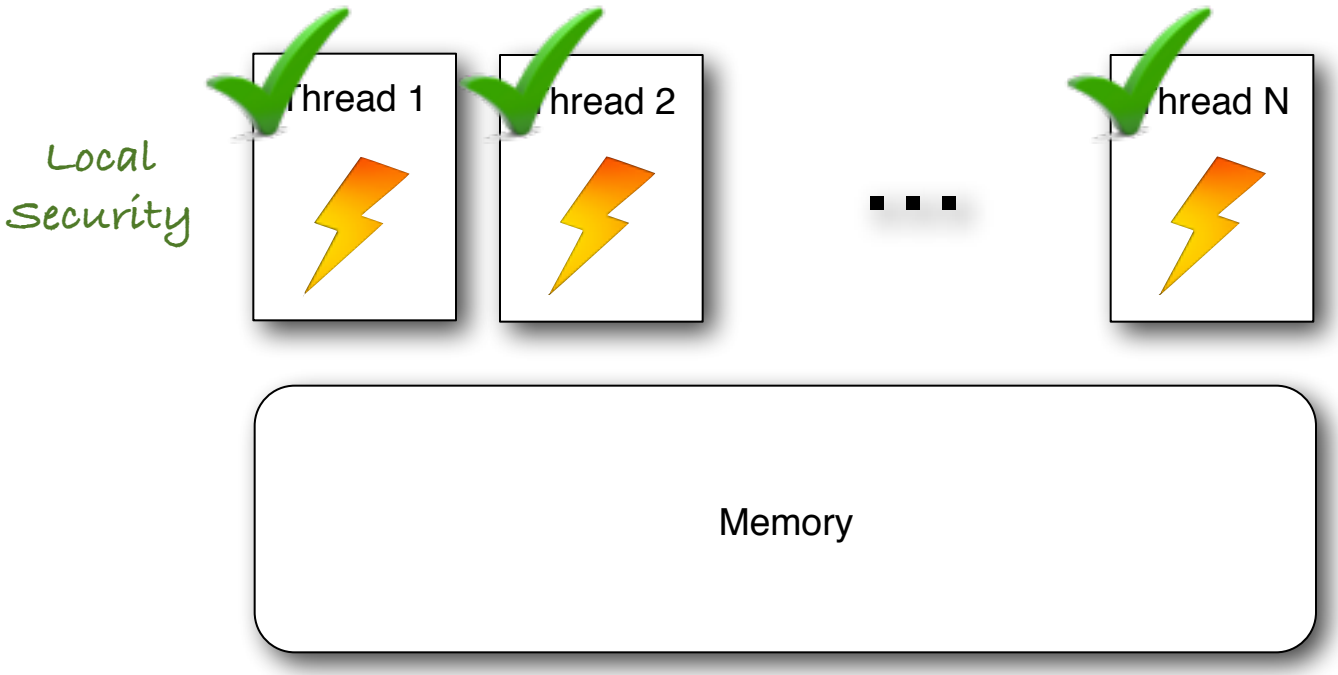
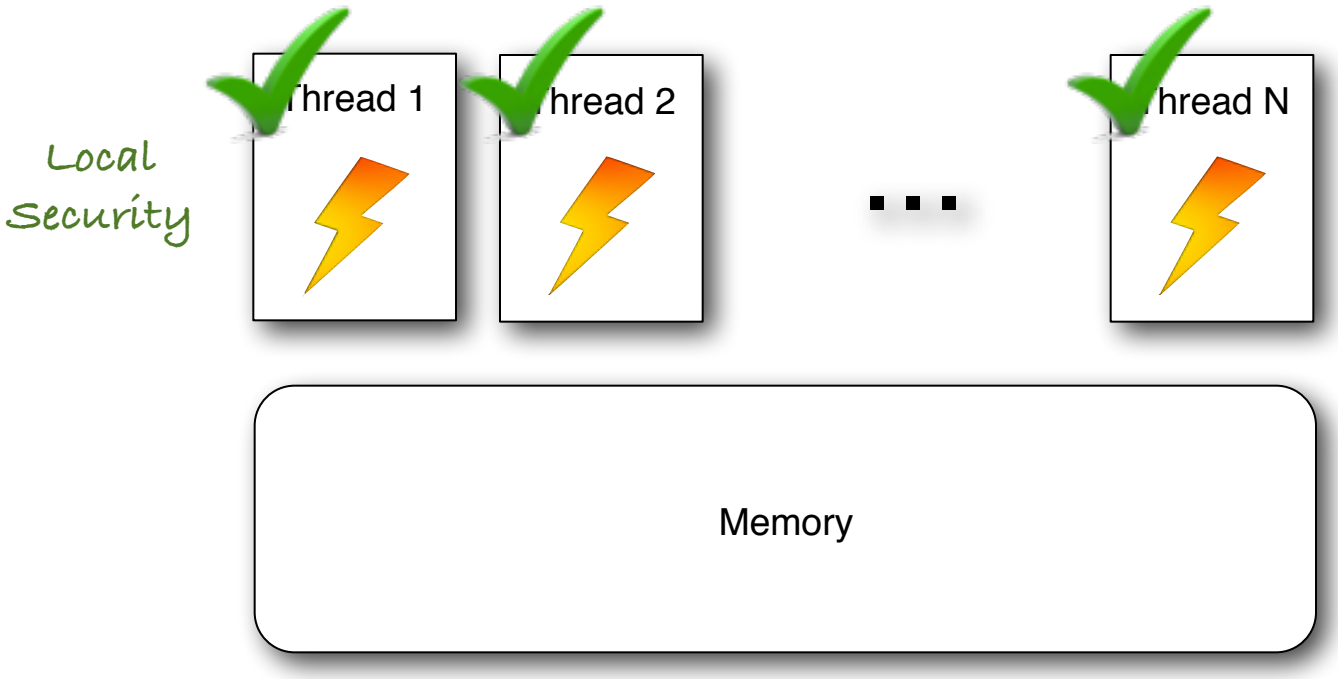


Each thread adheres to its own guarantees

Compositionality Theorem



Each thread adheres to its own guarantees

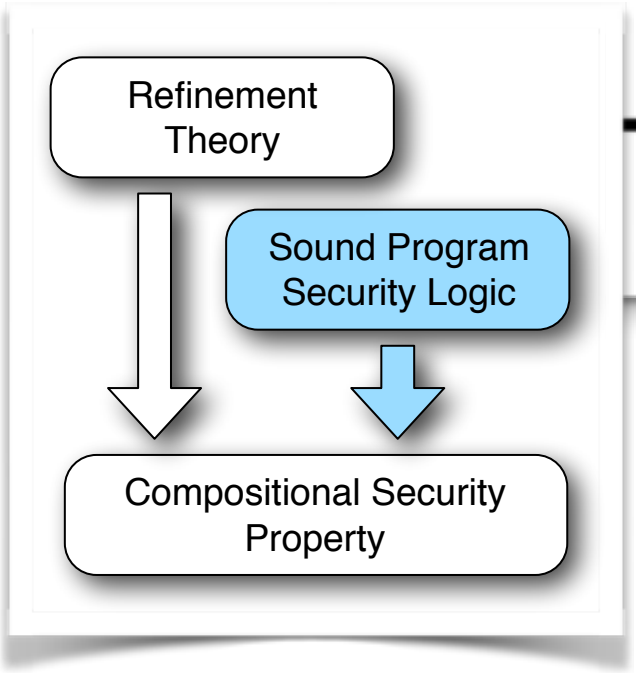
Each thread guarantees the assumptions of all others, at the right times

Compositionality Theorem

DEPENDENT SECURITY LOGIC

$$\Gamma \vdash e : t$$

DEPENDENT SECURITY LOGIC



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cmd ::= **skip**
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R = {(s,s'). global_invariant s → global_invariant s'}

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R = {(s,s'). global_invariant s → global_invariant s'}

this is also the global, never changing guarantee condition for everyone

Types and Typing Judgements

$$\vdash \Gamma, \mathcal{S}, P \ \{c\} \ \Gamma', \mathcal{S}', P'$$

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typing context

Types and Typing Judgements

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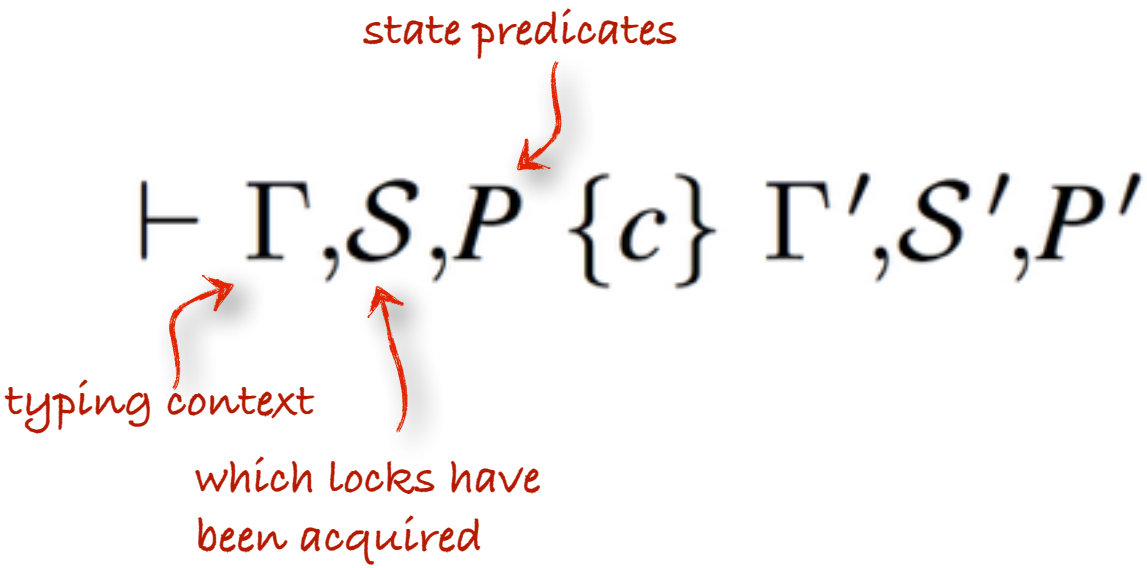
typing context

which locks have been acquired

Types and Typing Judgements



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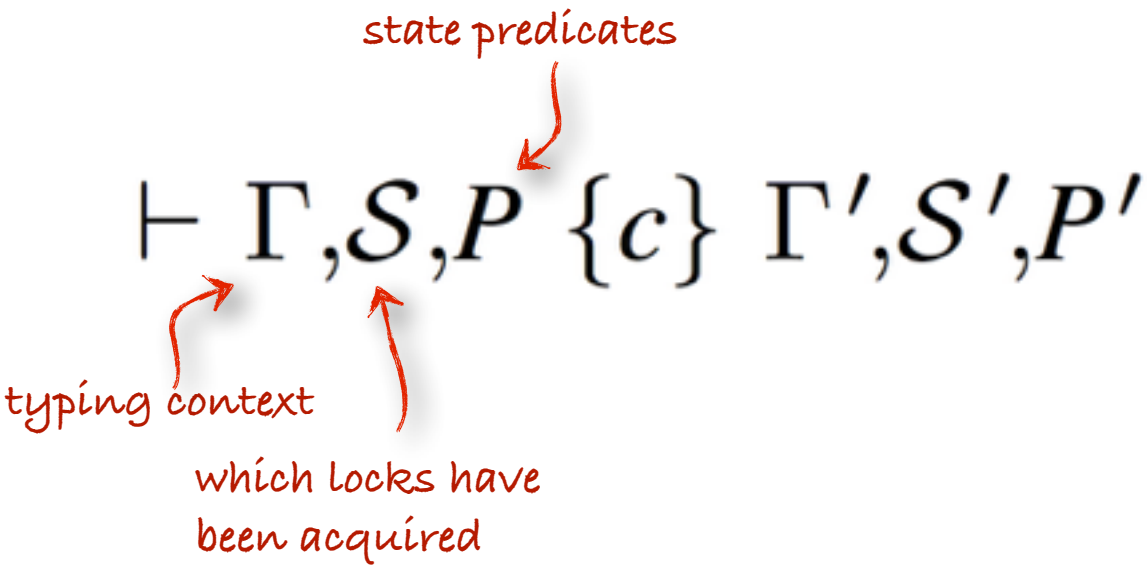

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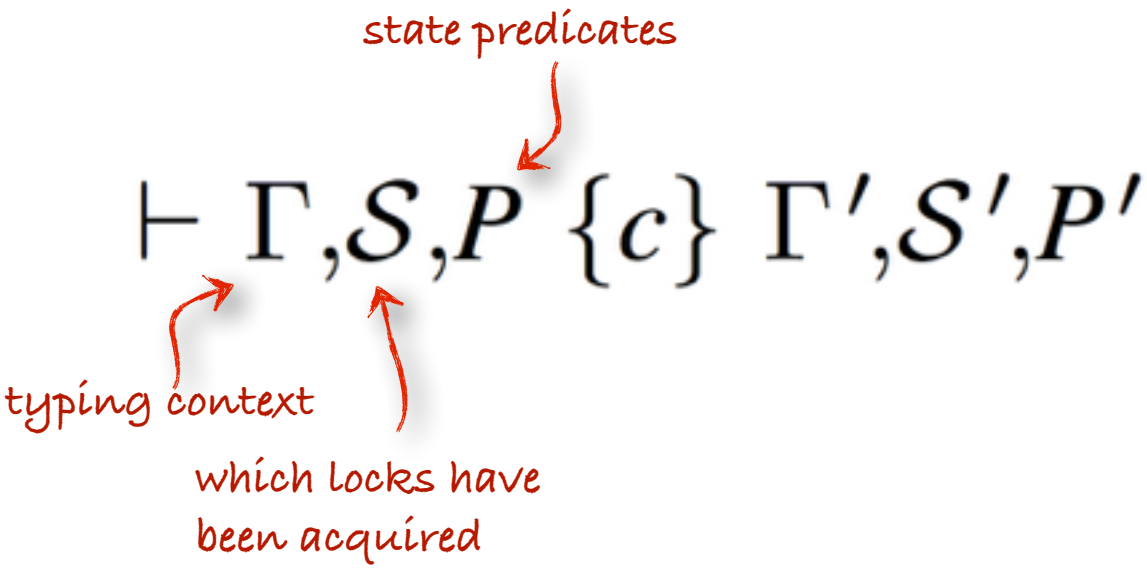
Types and Typing Judgements



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we encode them as (sets of) state predicates

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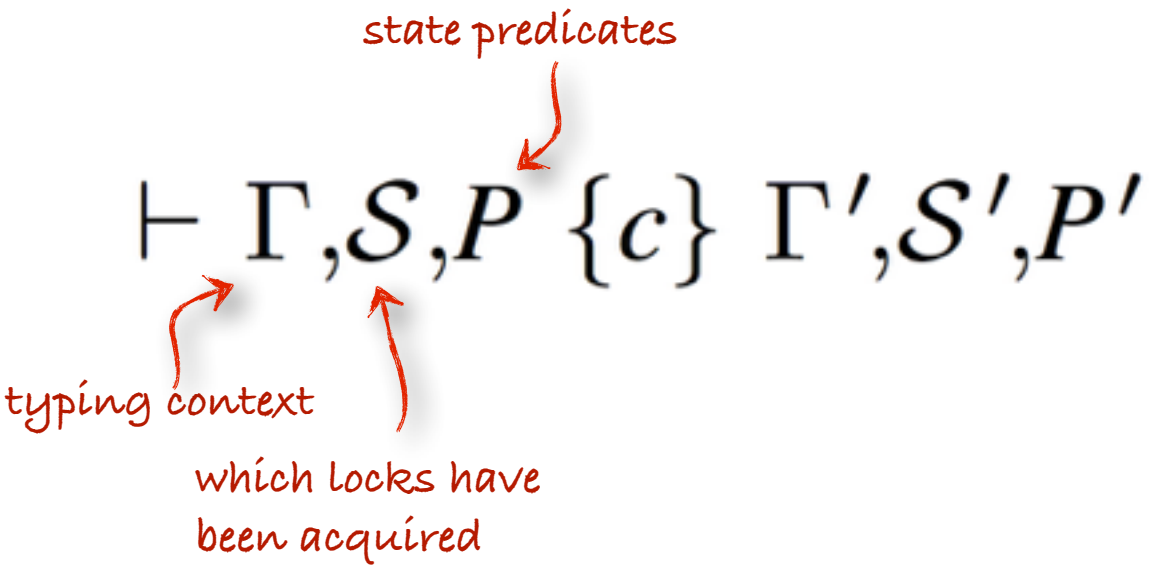

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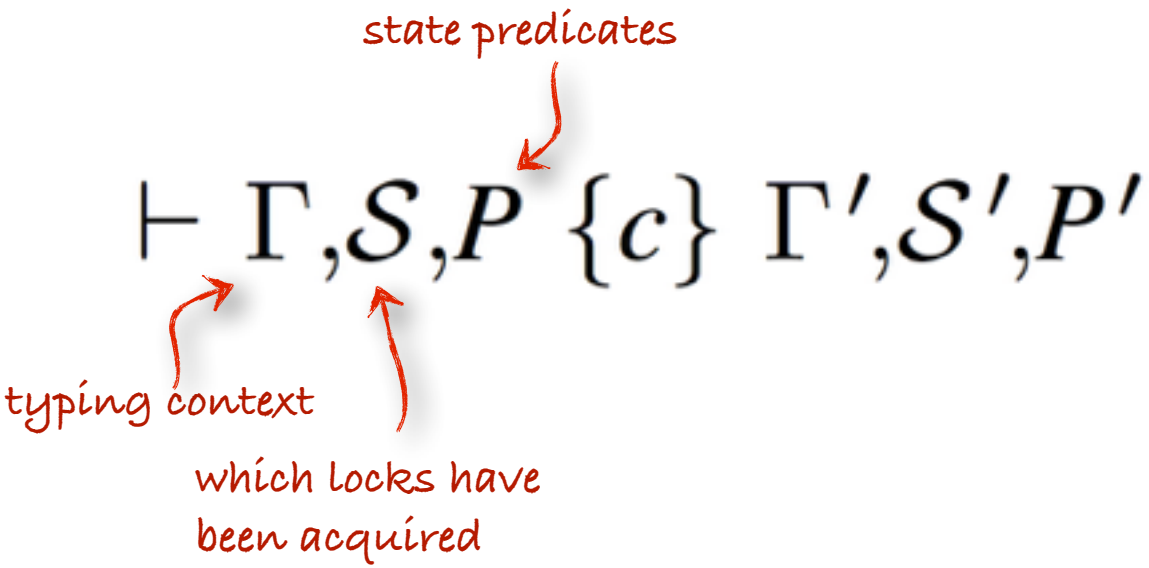

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subtype: $t \leq :_P t' \equiv (P \cup t') \vdash t$

Type System: Example in Action

```
lock(l);

temp := buffer;

if sMode == 0 then

  low-var := temp

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```

lock l protects `sMode`, `dMode` and `temp`, with invariant `sMode` = `dMode`

Type System: Example in Action

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Type System: Example in Action

[t : {dM=0}] {l} {sM=dM, sM=0}

$\Gamma \quad \mathcal{S} \quad P$

```
lock(l);
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Is {dM=0} a subtype of {}, under {sM=dM, sM=0} ?

lock l protects `sMode`, `dMode` and `temp`, with invariant `sMode` = `dMode`

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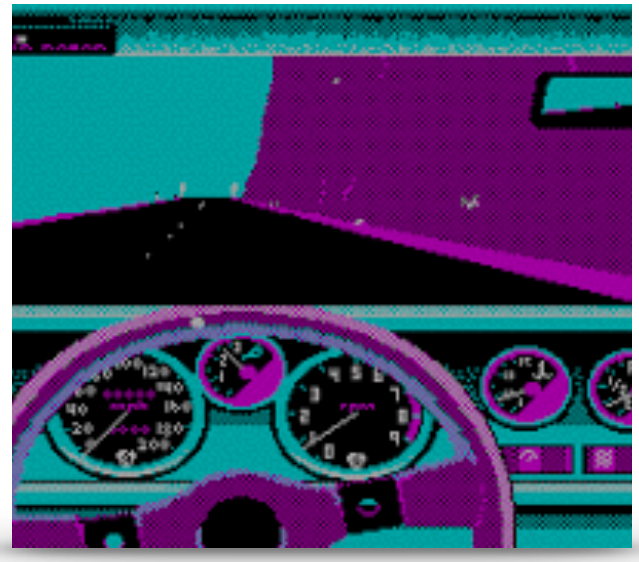
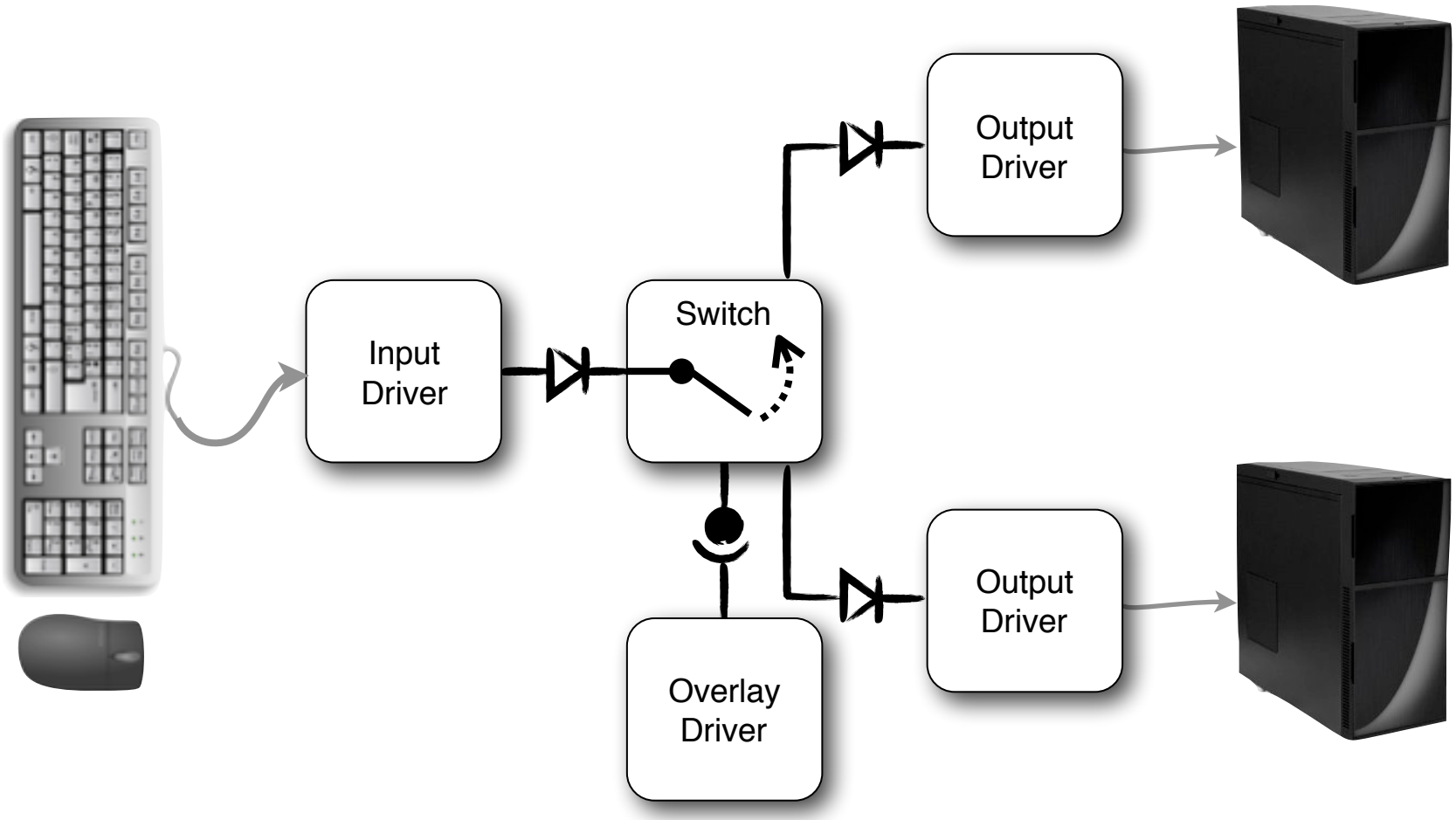
Status

- Soundness proof: almost complete
- Application to CDDC model: in progress

TEST-DRIVING THE FRAMEWORK

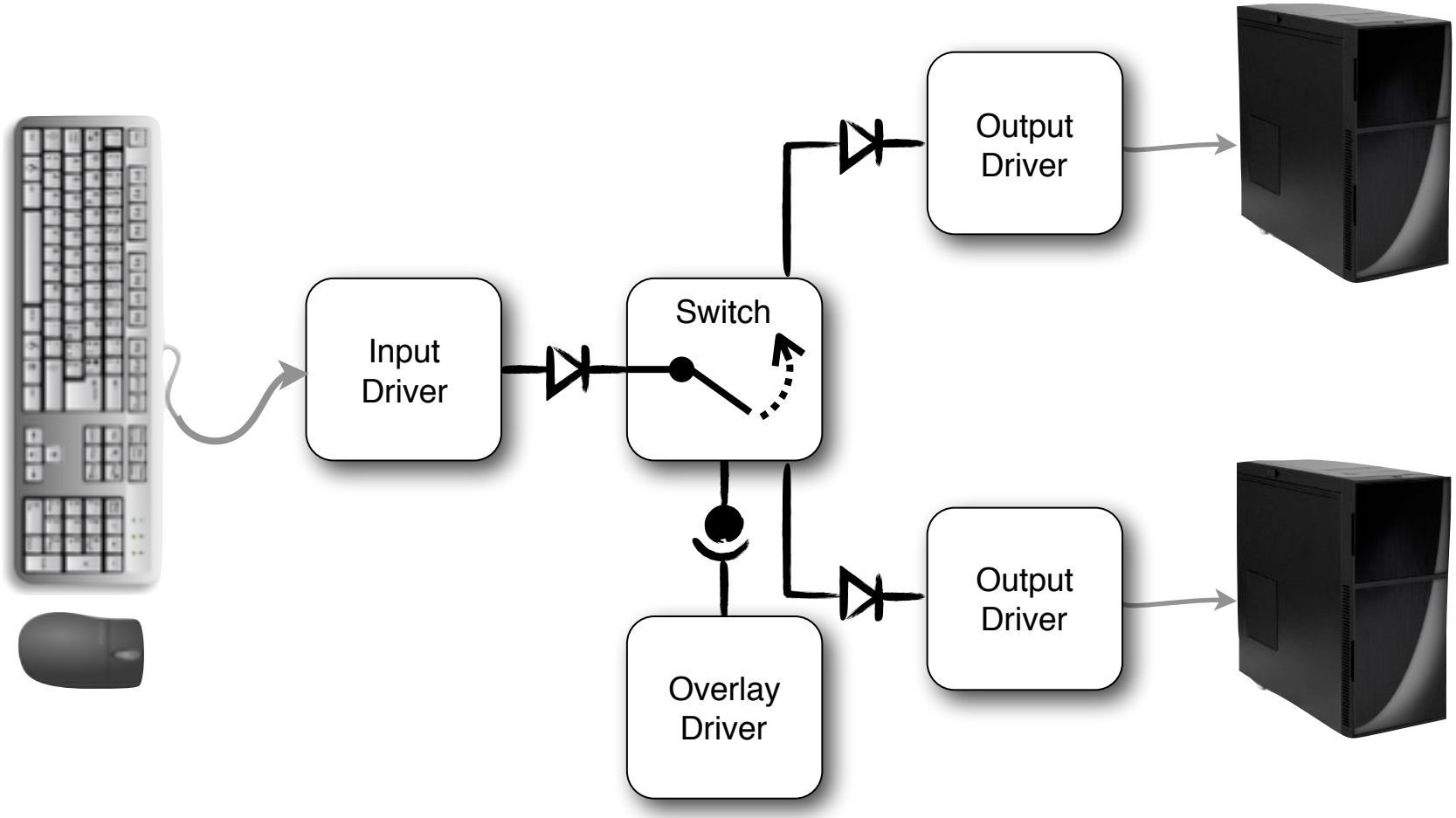


CDDC seL4-Based Software Architecture

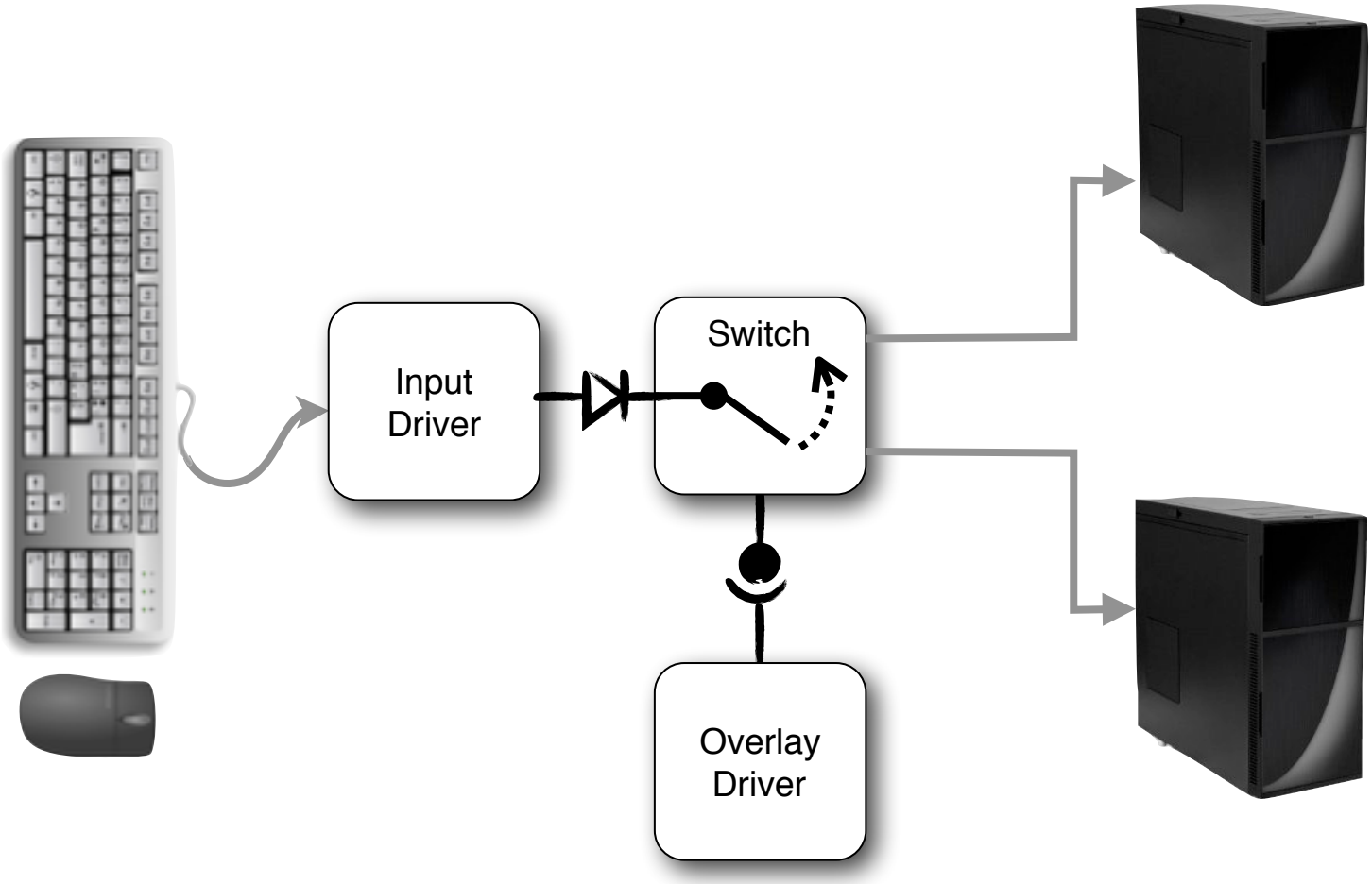


CDDC seL4-Based Software Architecture

(ignoring device administration and configuration, plus keyboard LED control)



(Almost) Verified CDDC Software



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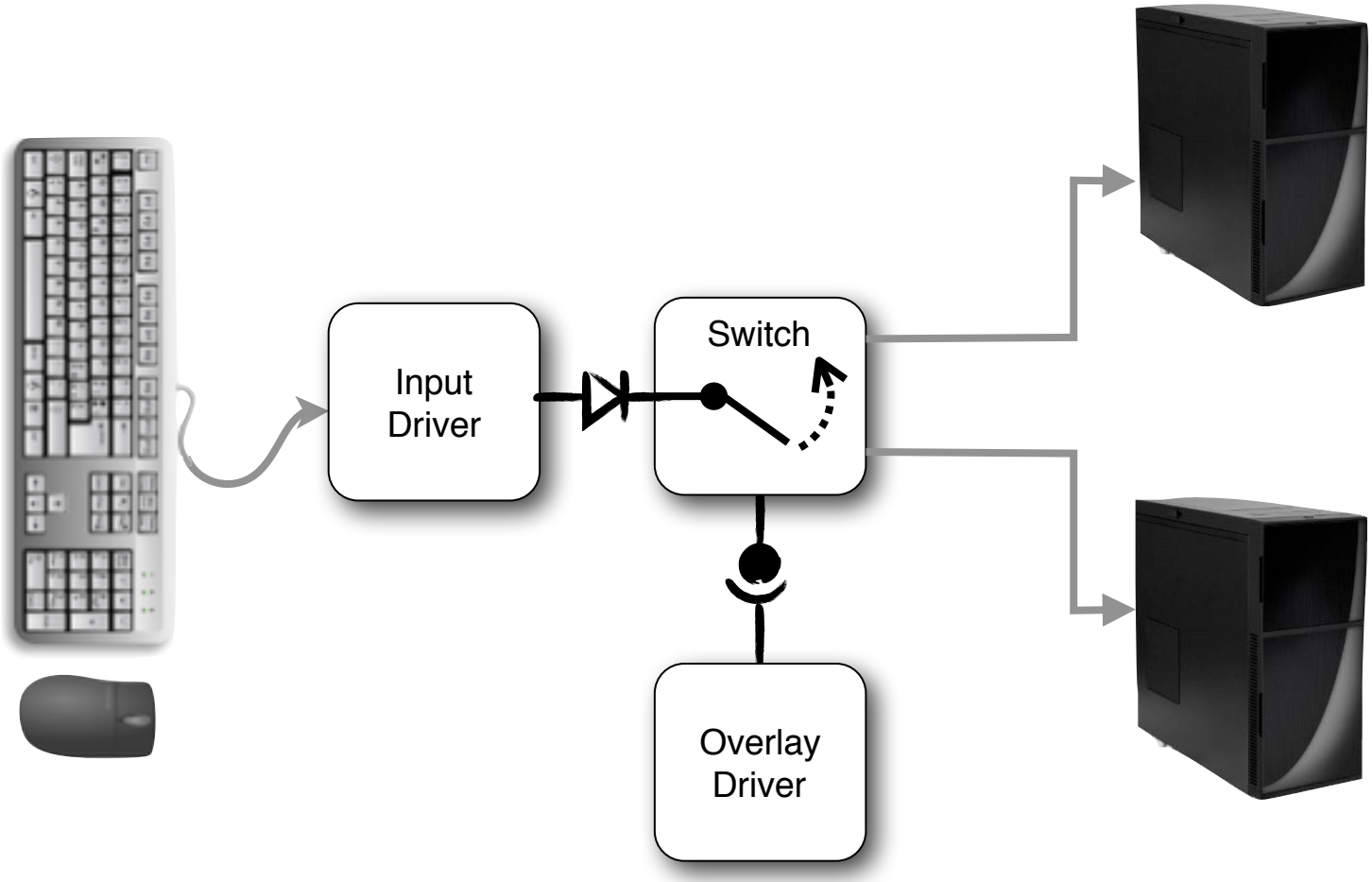
(static config, no hotkeys)



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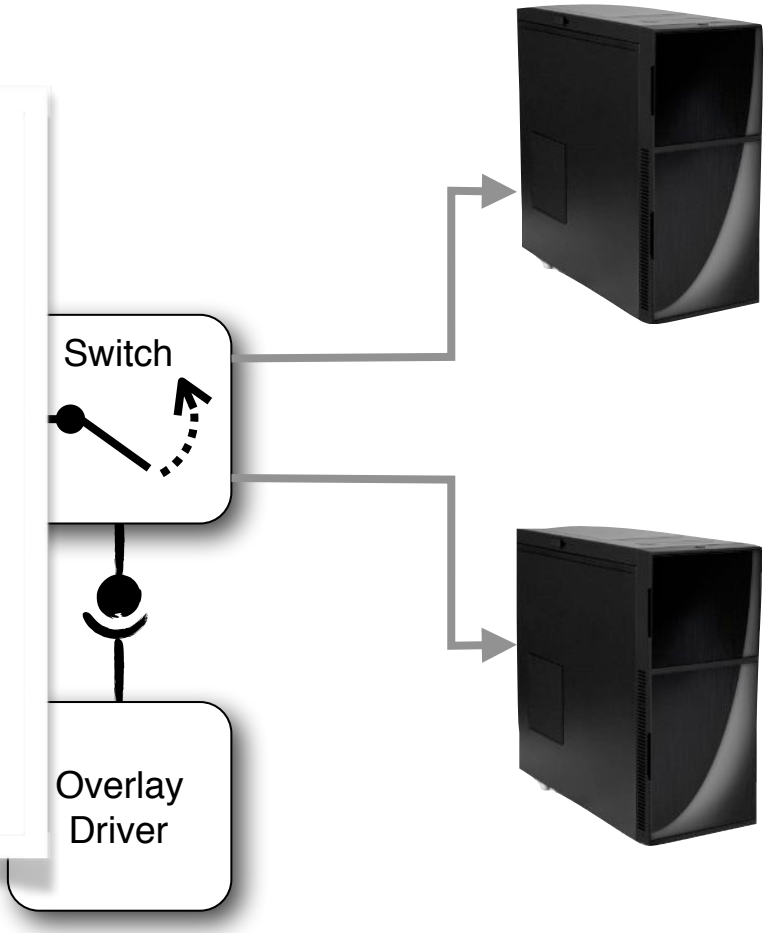
Makes use of:

- Value-dependent classification
- Shared-memory concurrency
- Lock-based synchronisation
- Inter-component invariants



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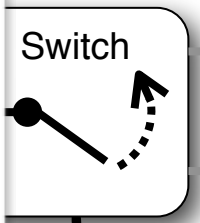

Avoids:

- Arrays & Pointer arithmetic
- Complex data structures

Pointers etc.

```
void write_labeled_val(int v, bool b,
                       int* highptr, int* lowptr) {
  if (b) {
    *highptr = *highptr | v;
  } else {
    *lowptr = *lowptr | v;
  }
}
```

Security Aware Separation Logic (c.f. Costanzo & Shao, POST 2014)

Pointers etc.

$$\{\texttt{highptr} \overset{\text{Hi}}{\longmapsto} h * \texttt{lowptr} \overset{\text{Lo}}{\longmapsto} l * [\texttt{b} = b, \texttt{v} = v, \texttt{b} :: \text{Lo}, \texttt{v} :: (b\ ?\ \text{Hi} : \text{Lo})]\}$$

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Pointers etc.

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Samuel Gruetter

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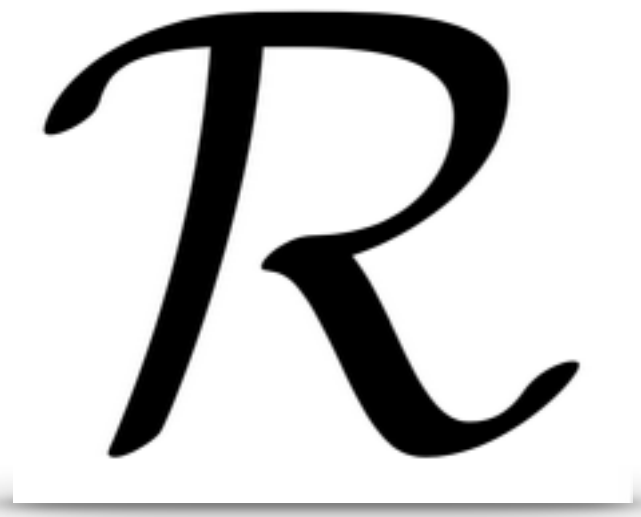
COMPOSITIONAL REFINEMENT



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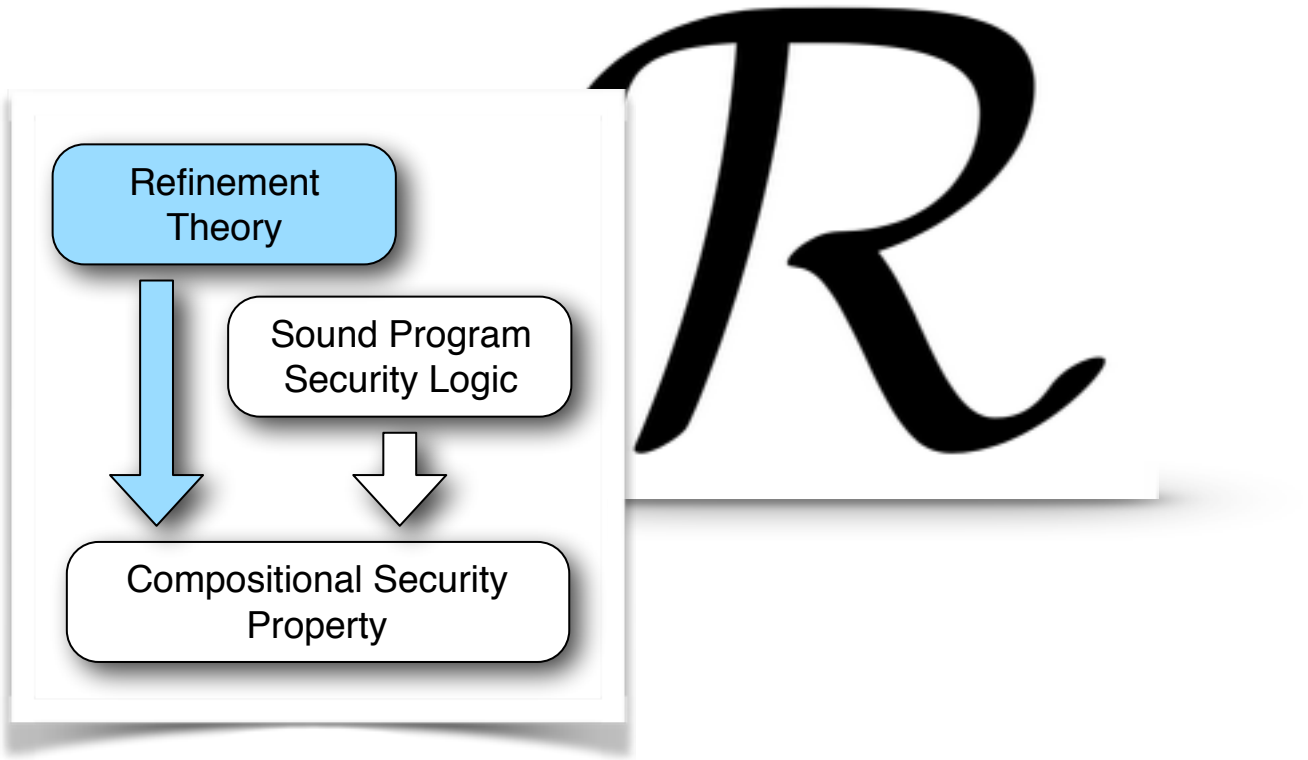
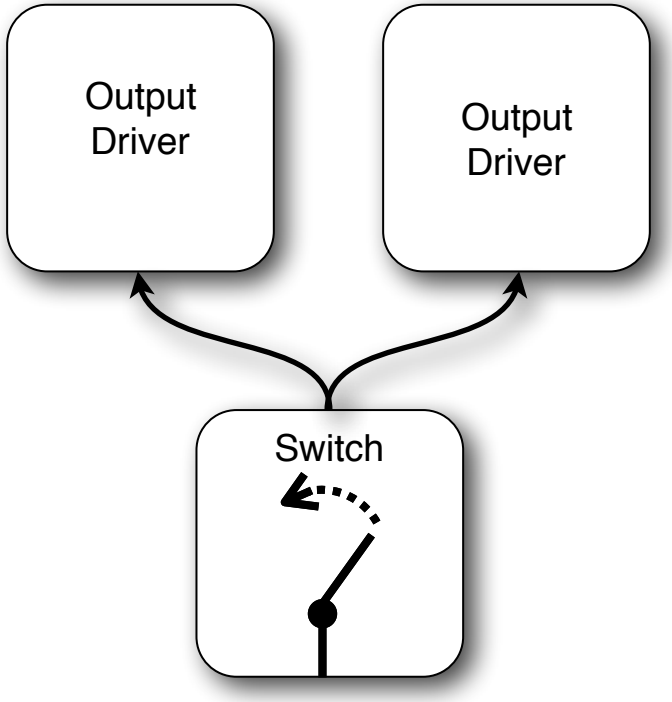


Secure Componentwise Refinement



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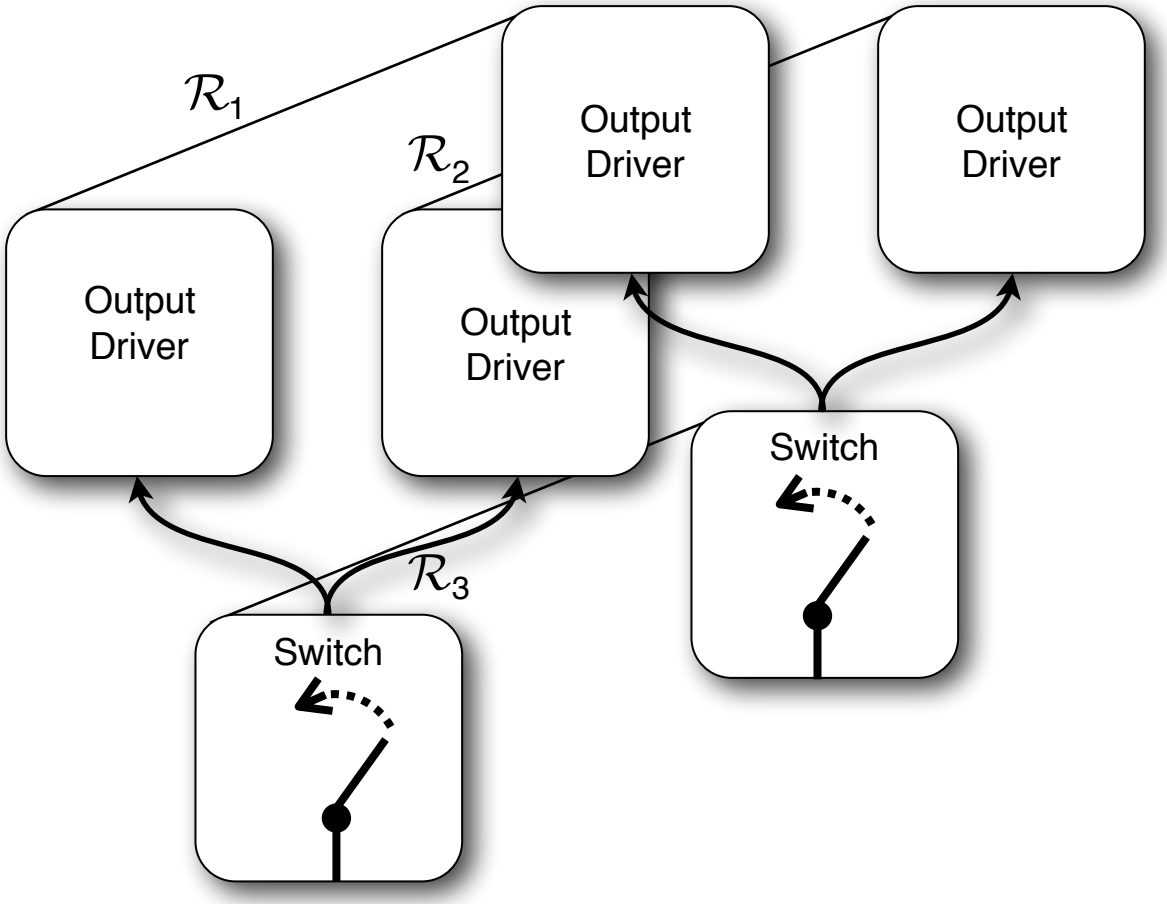

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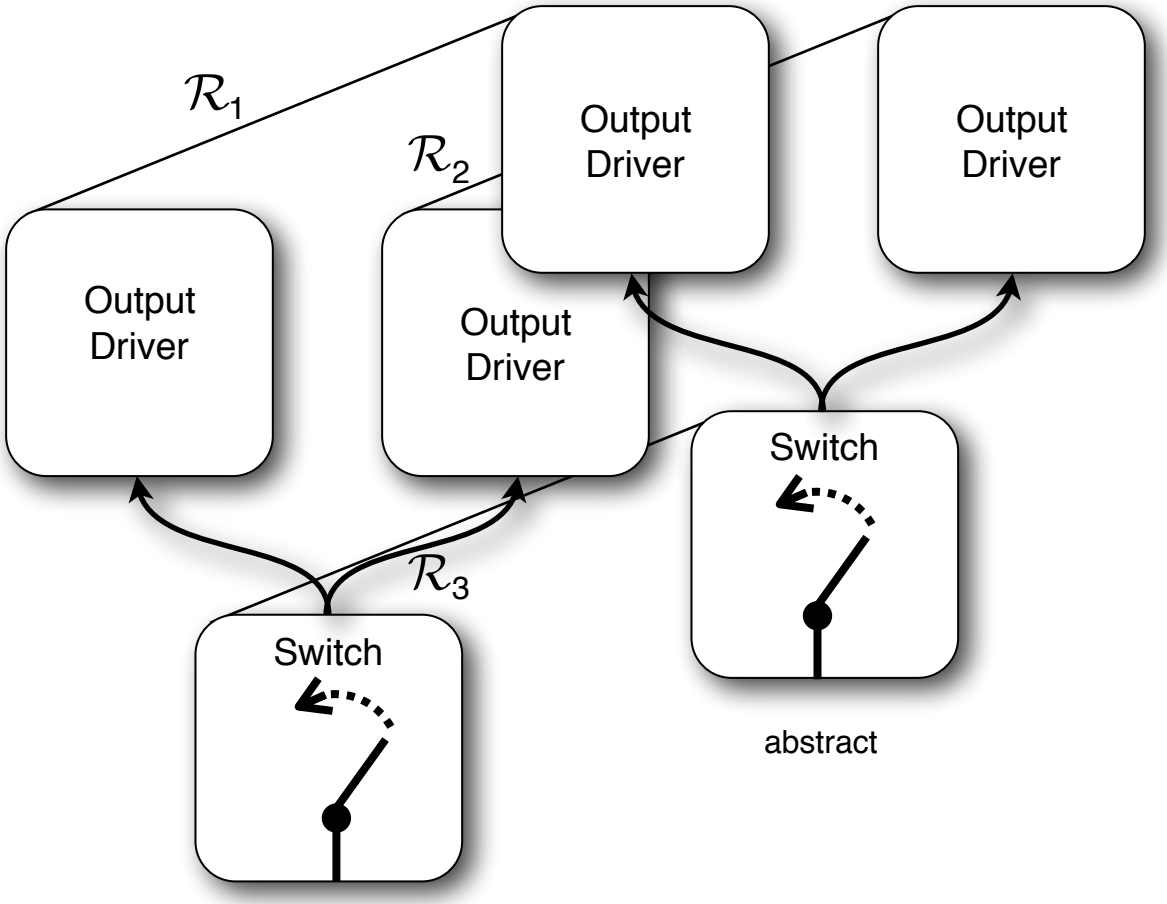

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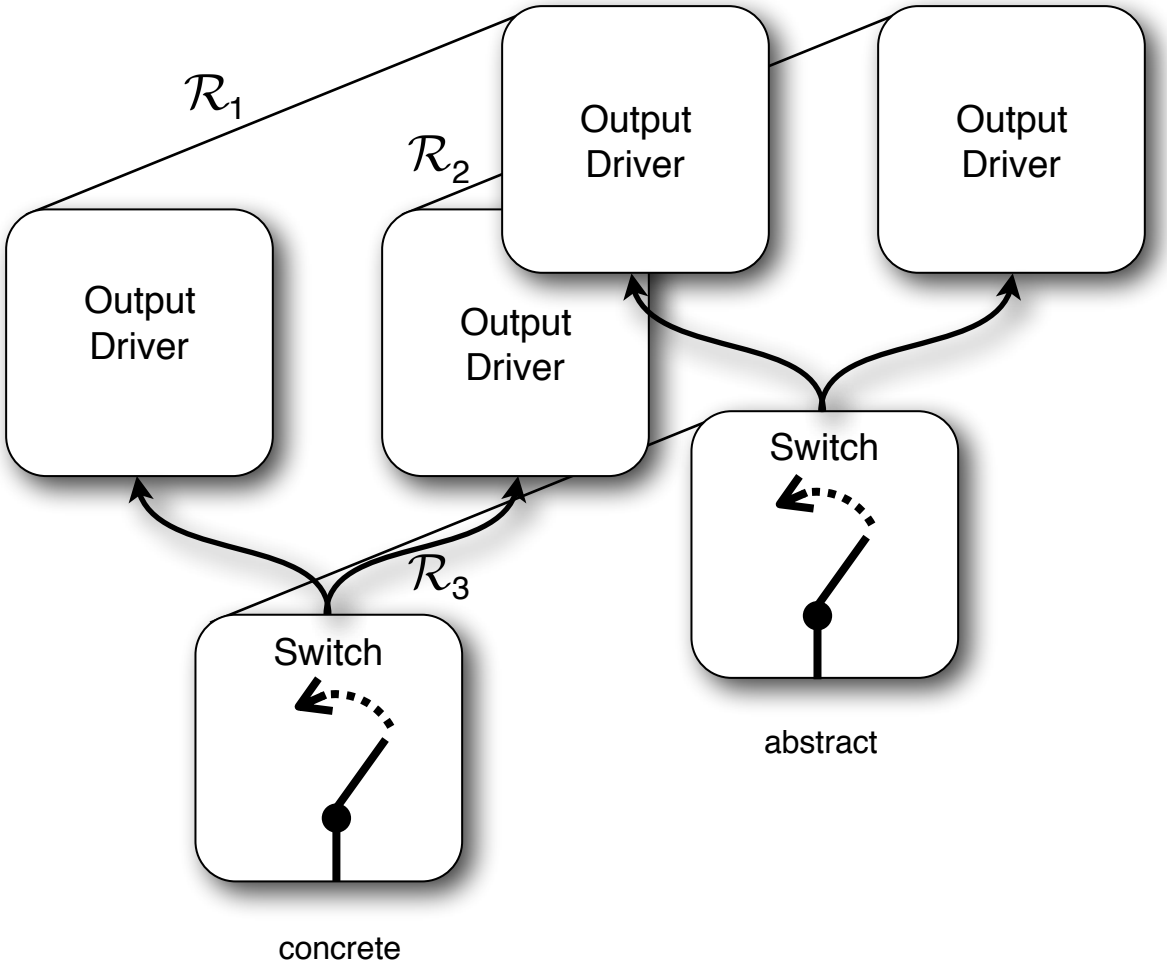

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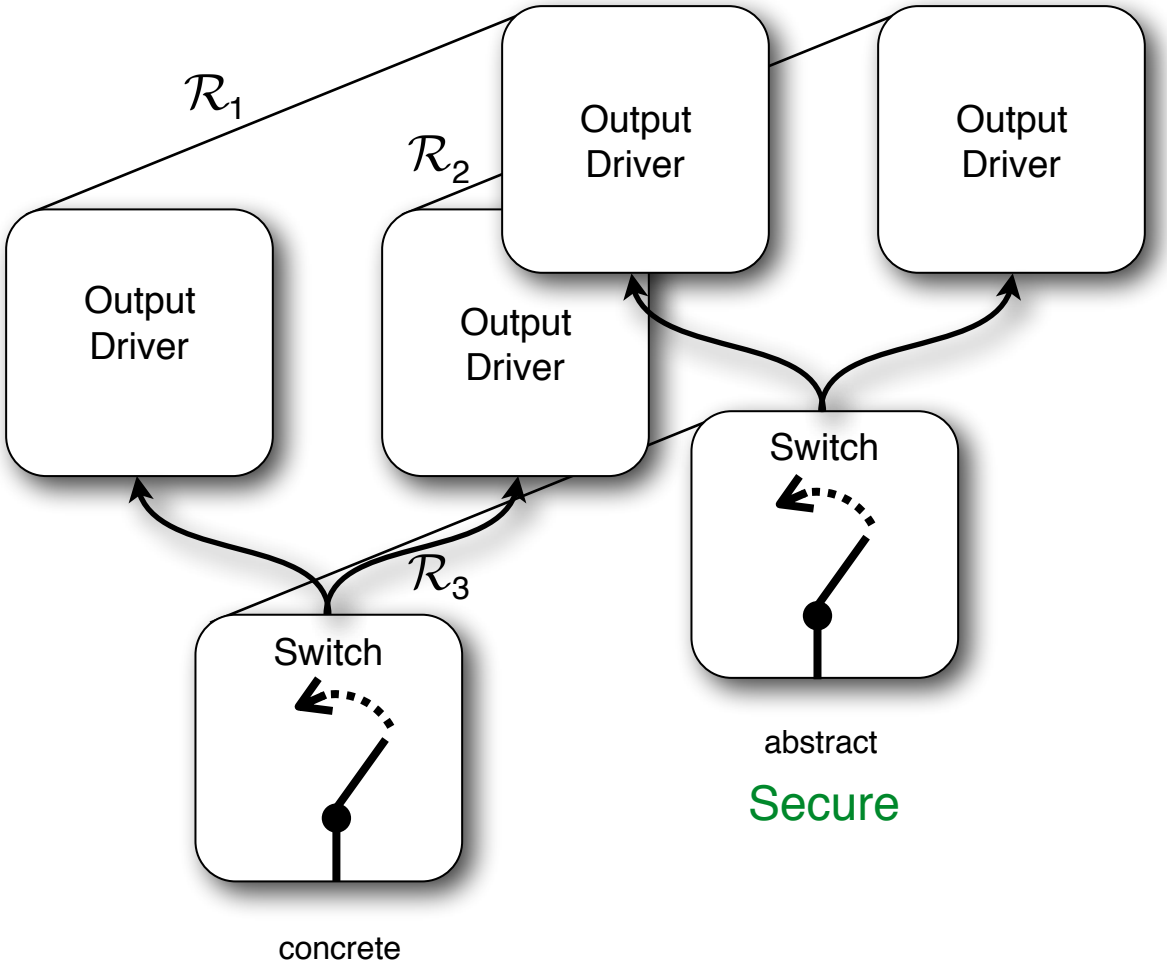

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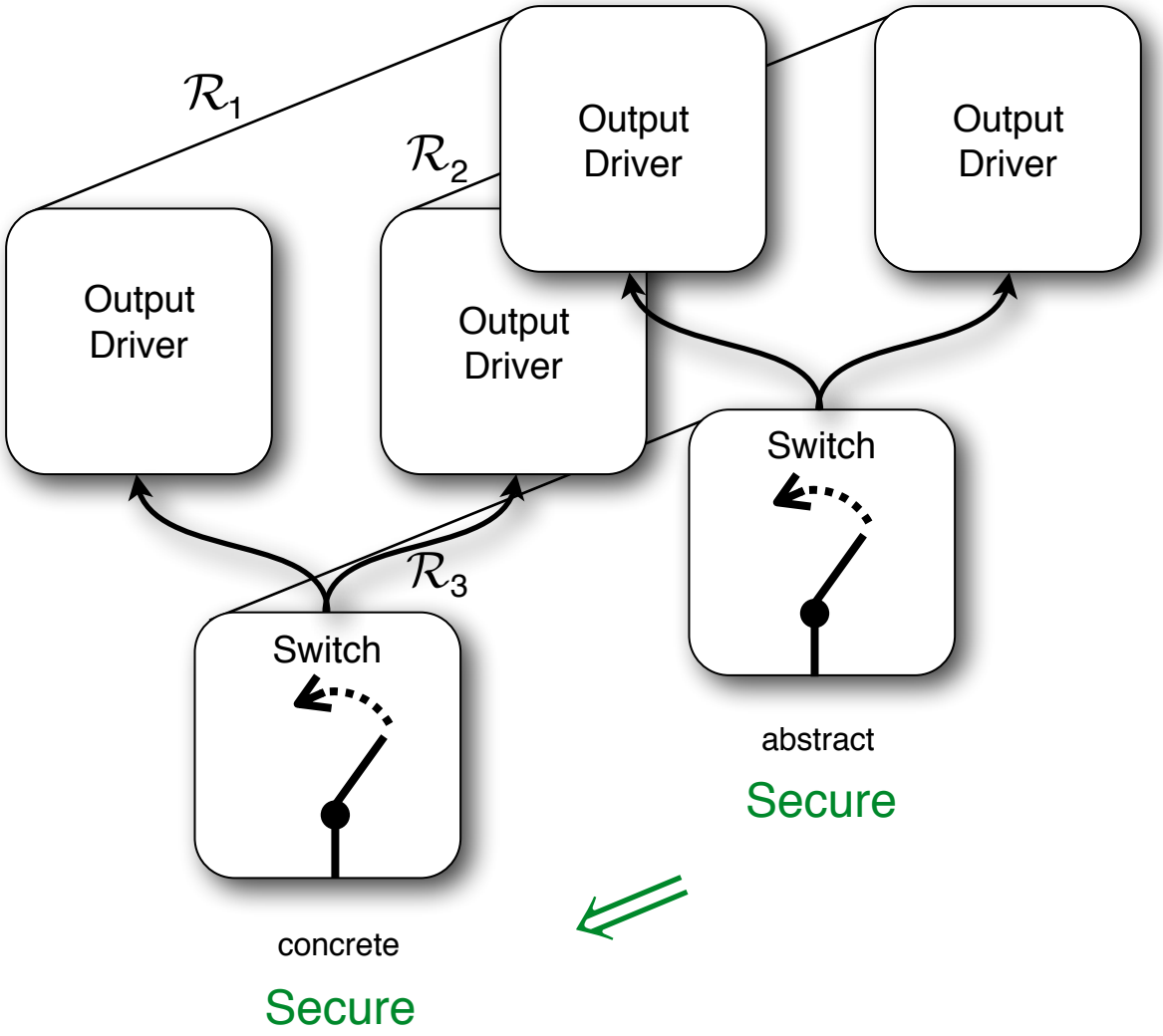

Component Refinement

```
skip   /* control +=_m AsmNoW */;
skip   /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
  low-var := temp
else
  high-var := temp
endif;
temp := 0;
skip   /* temp -=_m AsmNoRW */
```

```
skip   /* control_C +=_m AsmNoW */;
skip   /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
  low-var_C := temp_C
else
  high-var_C := temp_C
endif;
temp_C := 0;
skip   /* temp_C -=_m AsmNoRW */
```

Component Refinement

Original Program

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skip   /* control +=_m AsmNoW */;
skip   /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
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A Trivial Refinement

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Component Refinement

concrete variables implementing abstract ones

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skip   /* temp -=_m AsmNoRW */
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skip   /* control_C +=_m AsmNoW */;
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reg_C := control_C;
if reg_C == 0 then
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Component Refinement

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skip  /* control +=_m AsmNoW */;
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if control == 0 then
  low-var := temp
else
  high-var := temp
endif;
temp := 0;
skip  /* temp -=_m AsmNoRW */
```

concrete variables implementing abstract ones

concrete variables with no abstract counterpart

A Trivial Refinement

```
skip  /* control_C +=_m AsmNoW */;
skip  /* temp_C +=_m AsmNoRW */;
temp_C := buffer_C;
reg_C := control_C;
if reg_C == 0 then
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endif;
temp_C := 0;
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Component Refinement

Original Program

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Abstract Program Security: Bisimulation

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$\mathcal{B}$ must guarantee that the two memories are always Low-equivalent

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```

(the soundness proof for the type system constructs an appropriate $\mathcal{B}$)

Important:

$\mathcal{B}$ must guarantee that the two memories are always Low-equivalent

Refining High Conditionals

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if (h) {
    h = 0;
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```

Refining High Conditionals

A Secure Program

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Refining High Conditionals

A Secure Program

branches need to do the same Low things at the same time

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```
if (h) {
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} else {
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}
```
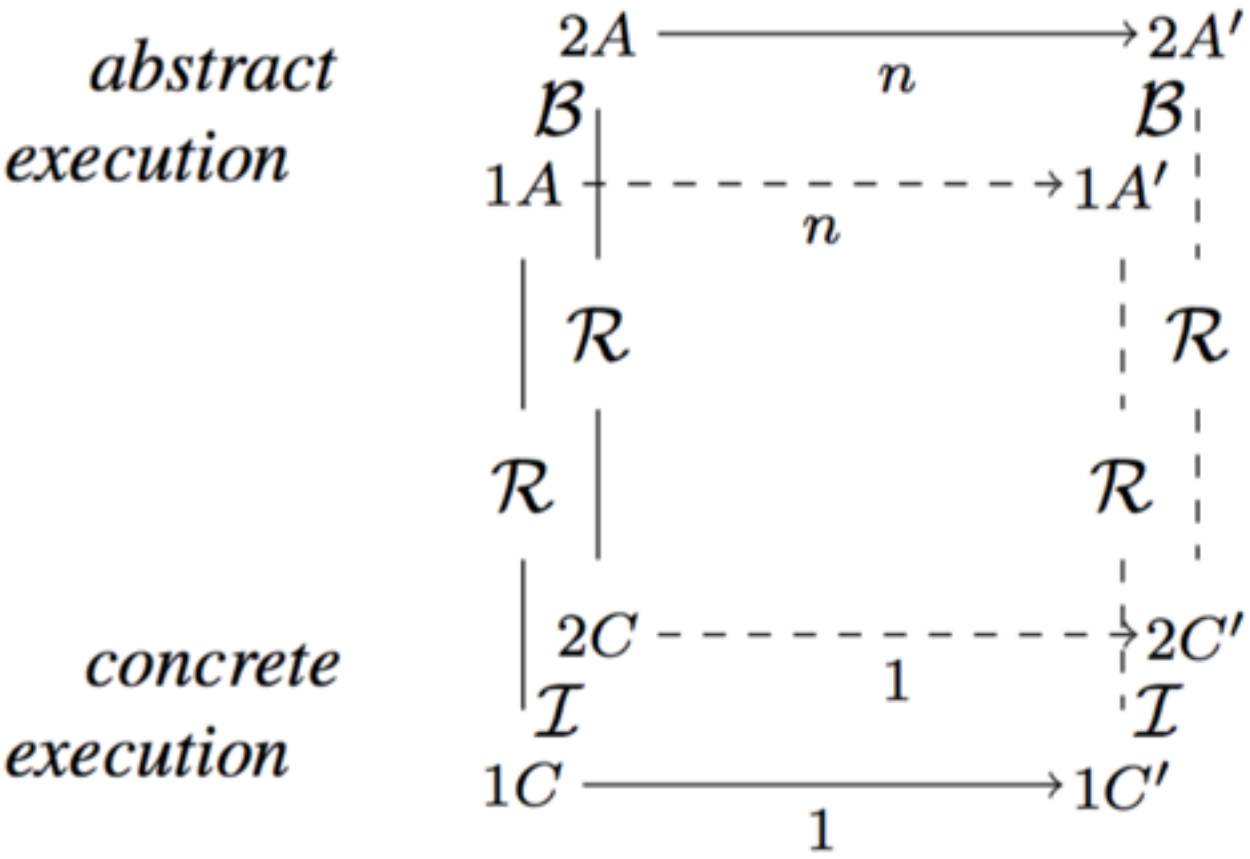
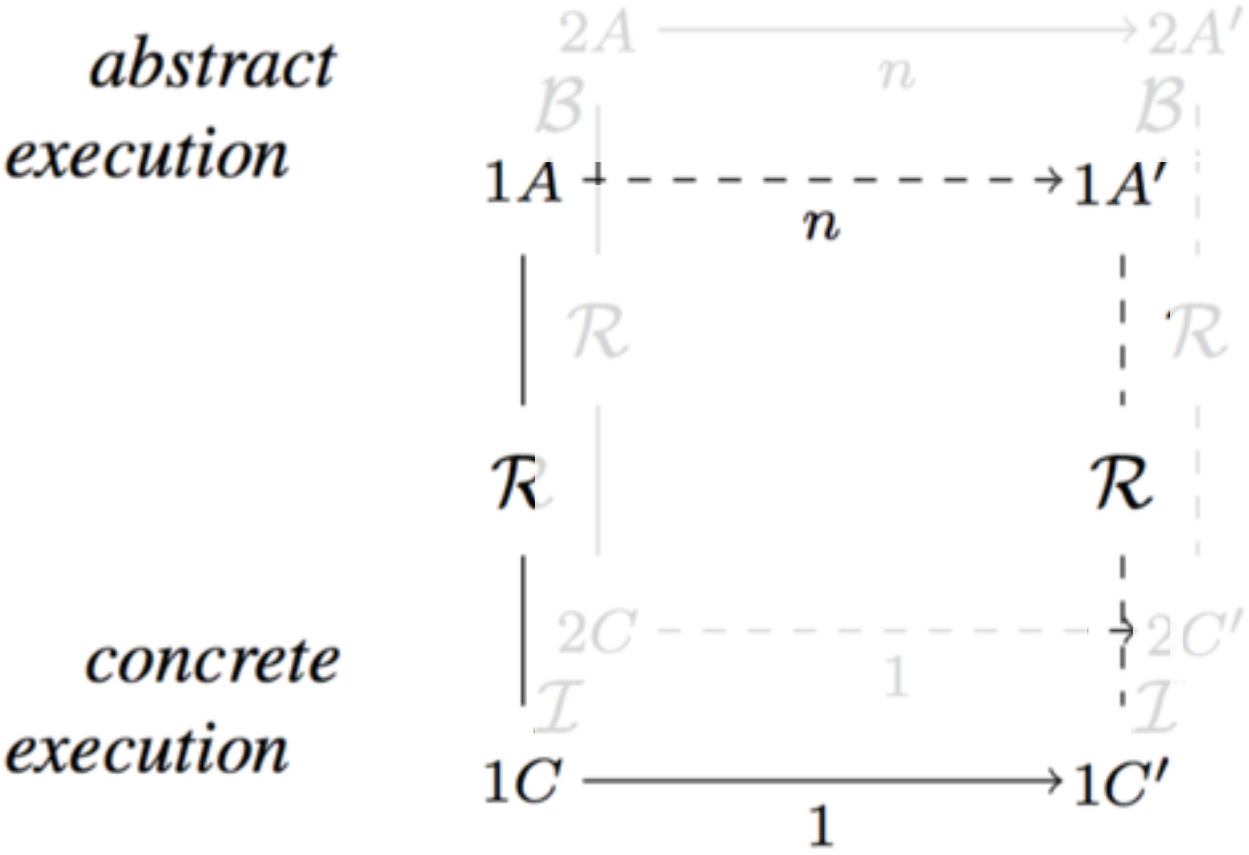

insecure

Need to make sure that the concrete executions stay in sync.

Secure Refinement via Coupling



Secure Refinement via Coupling



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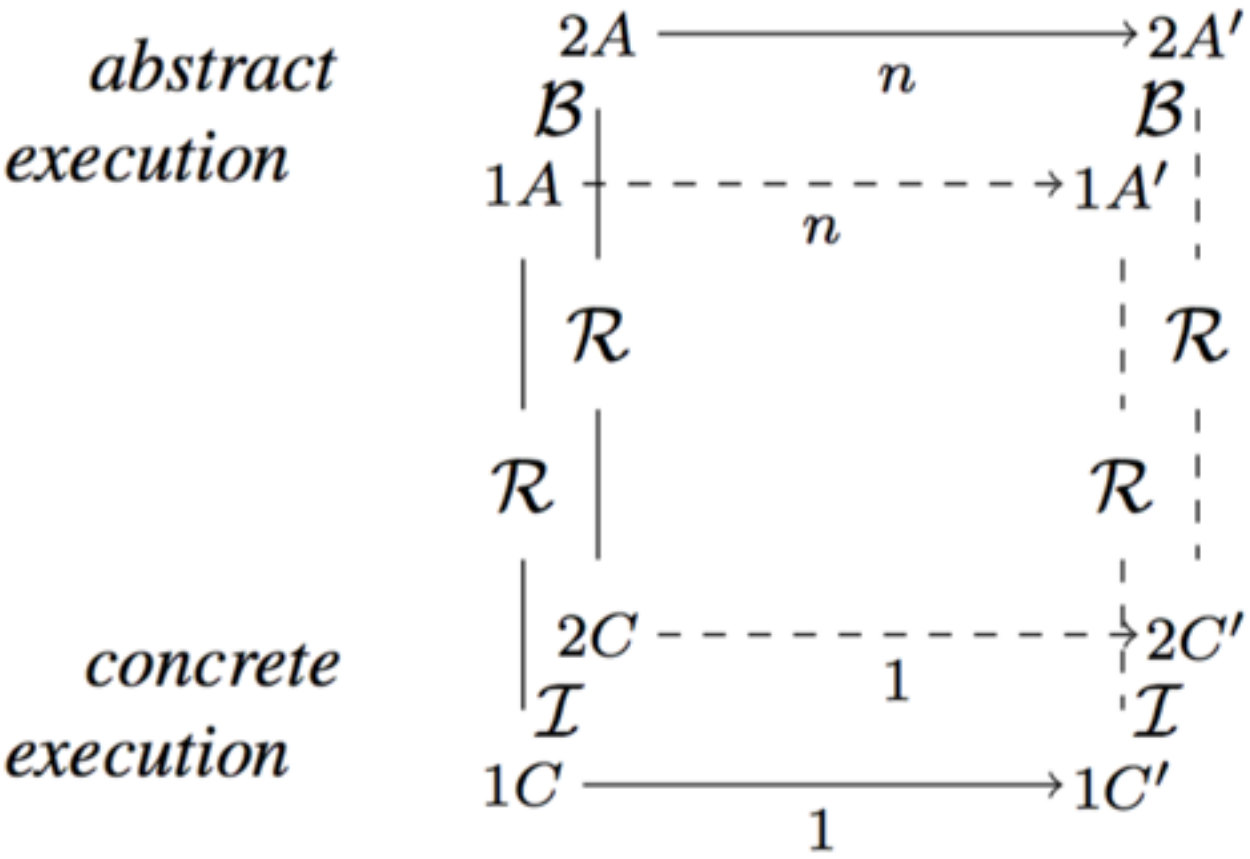

Coupling Invariant: $\mathcal{I}$

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Important:

$\mathcal{I}$ need not talk at all about memory contents being secure

Concurrency-Aware Refinement

$$x := y + z$$

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Source language semantics evaluates y + z atomically

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i.e. that the refinement relation is preserved by potential actions of other threads

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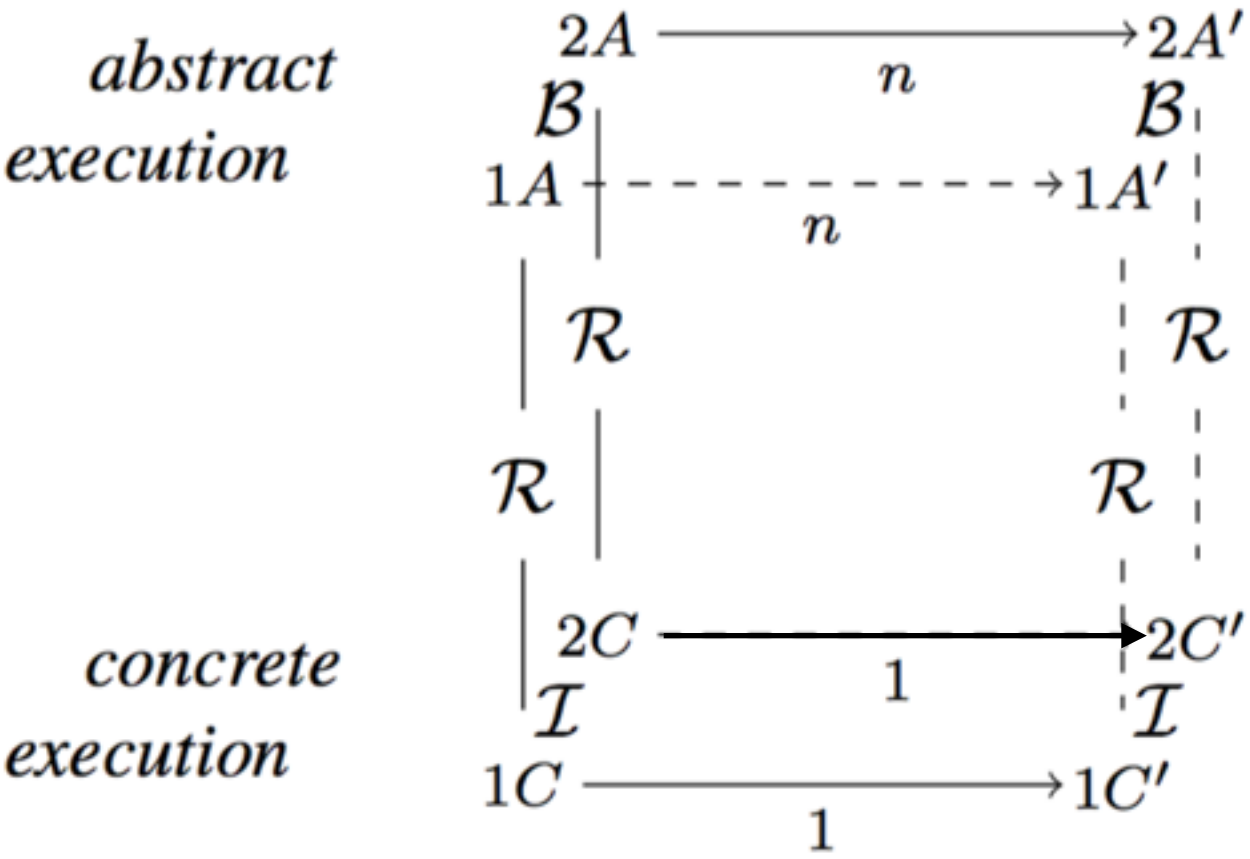
(see Liang et al., TOPLAS 2014)

i.e. that the refinement relation is preserved by potential actions of other threads

Leveraging Determinism



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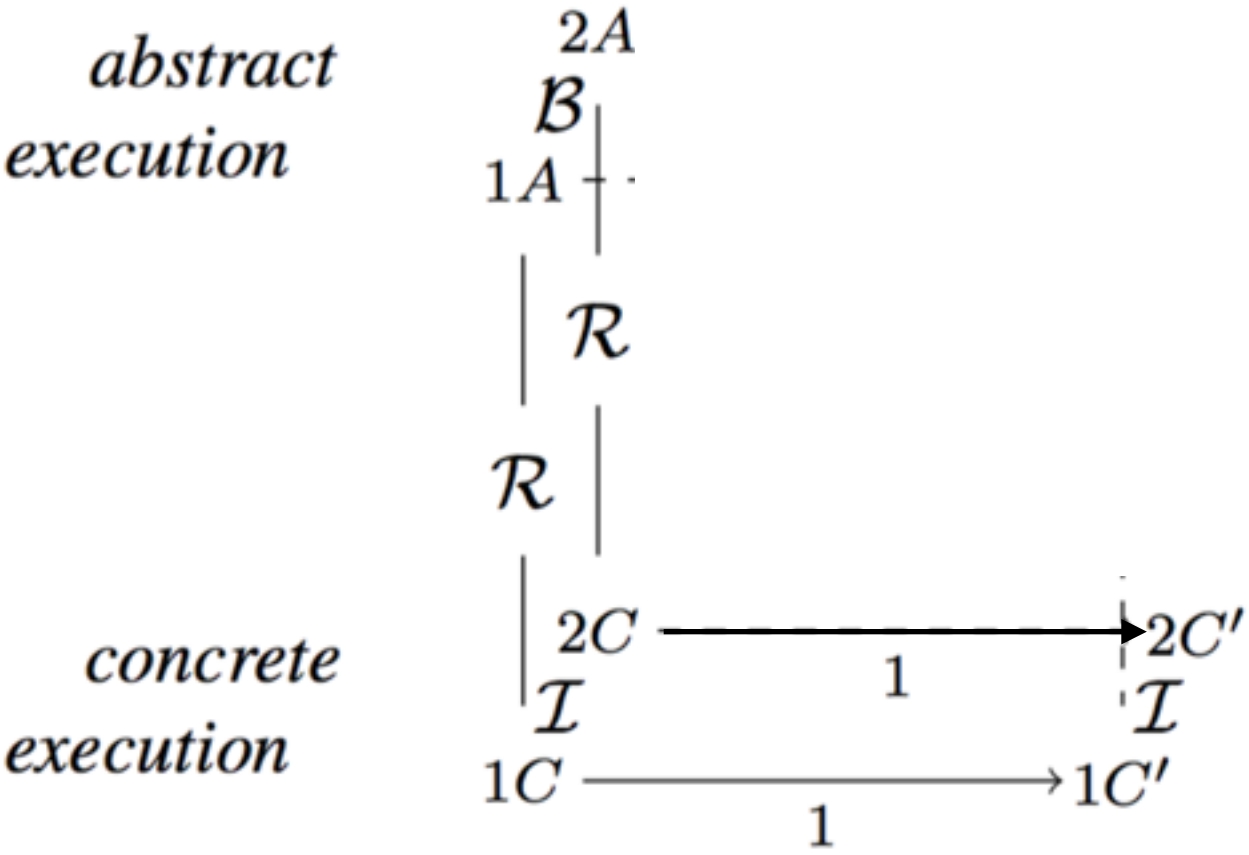

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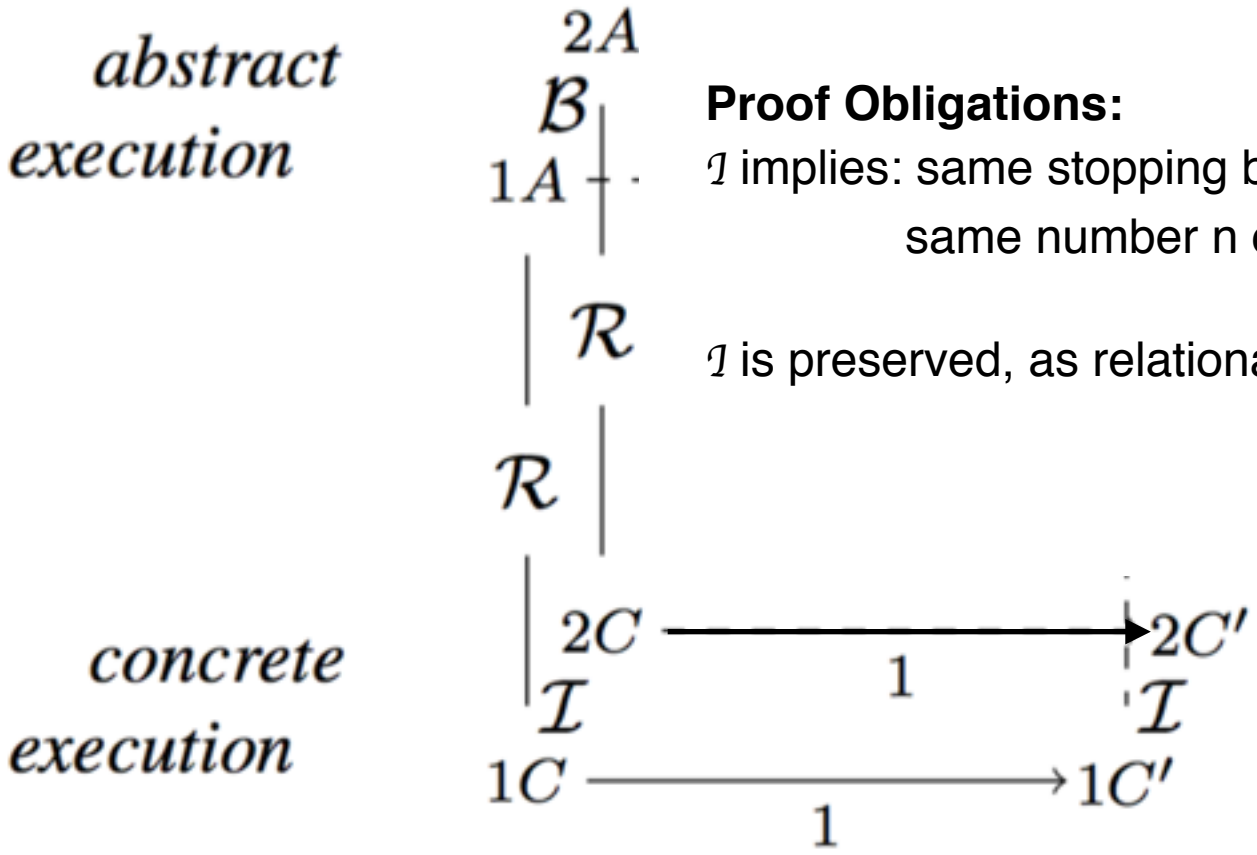

Proof Obligations:

$\mathcal{I}$ implies: same stopping behaviour
same number n of abstract steps

$\mathcal{I}$ is preserved, as relational invariant

SECURITY-PRESERVING COMPILATION

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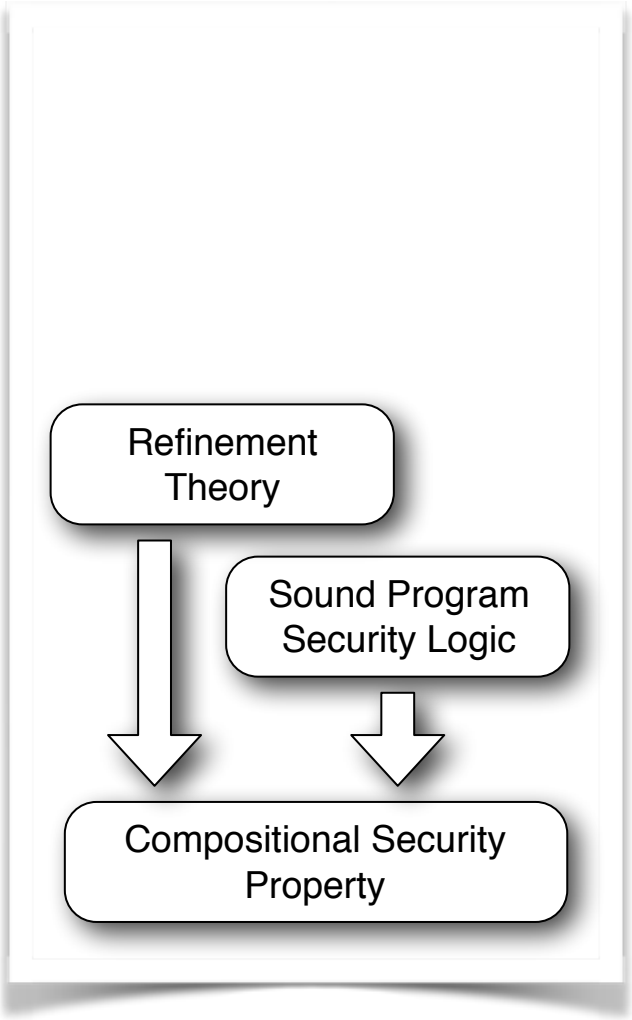

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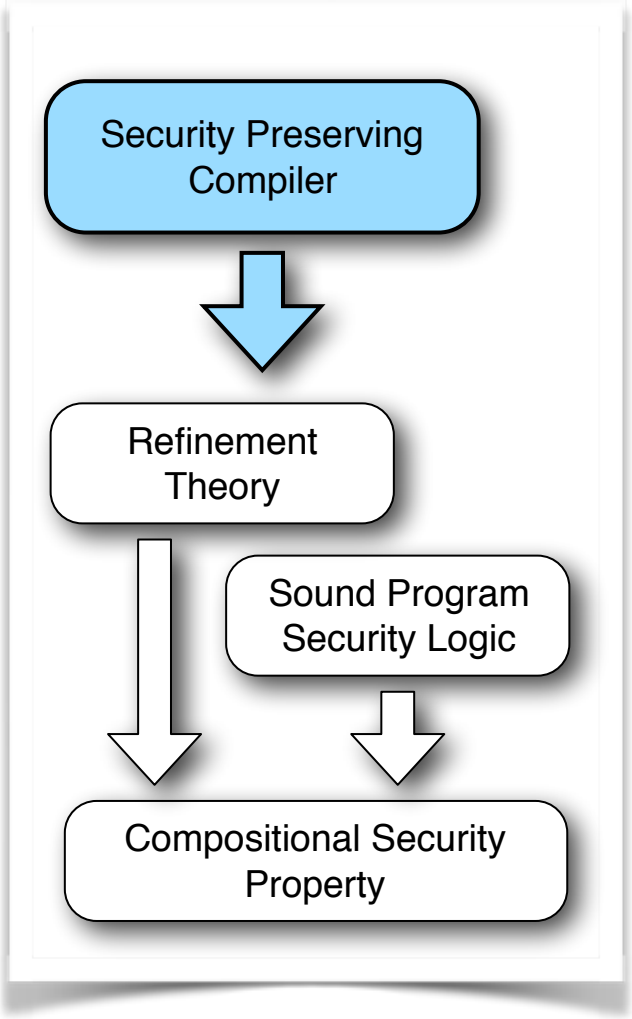

Case Study: Compilation to Idealised RISC

instr ::= **lock** l
| **release** l
| **load** reg x
| **store** x reg
| **Jump** label
| **Jz** label
| **Noop**
| **MoveK** reg w
| **Mov** reg reg
| **Binop** op reg reg

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MoveK reg w
Mov reg reg
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Robert Sison

Current Status

- Proof finished for source programs that are secure and never branch on High data
  - This is the simple case where the compiler doesn't have to do anything except compile the program properly to preserve noninterference
- Sufficient for the CDDC model we have verified
- First example compiler for shared-memory concurrent programs proved to preserve noninterference
- Next steps: High conditionals, weak memory, …

How to leverage it?

- Constant-time RISC simulator for concurrent programs
  - A mini RTOS/VM

CONCLUSION

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Moving from verified secure kernels to verified secure systems:

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Moving from verified secure kernels to verified secure systems:

- concurrency ~> compositionality ~>
  timing-sensitivity, assume-guarantee reasoning
- dynamic policies (value-dependence)
- compositional secure refinement ~>
  coupling invariants for preservation of timing-sensitive security

CONCLUSION

Moving from verified secure kernels to verified secure systems:

- concurrency ~> compositionality ~>
  timing-sensitivity, assume-guarantee reasoning
- dynamic policies (value-dependence)
- compositional secure refinement ~>
  coupling invariants for preservation of timing-sensitive security

Still lots more to be done.

Thank You


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@tobycmurray

Dependent Security Logic: Intuition

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inspired by Mantel et al. CSF 2011

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Dependent Security Logic: Intuition

inspired by Mantel et al. CSF 2011

buffer's classification depends on control: is Low iff control == 0

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buffer's *classification depends on* control: *is* Low *iff* control == 0

assume nobody else can modify control

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```

Dependent Security Logic: Intuition

inspired by Mantel et al. CSF 2011

buffer's *classification depends on* control: *is* Low *iff* control == 0

assume nobody else can read or modify temp

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buffer's *classification depends on* control: *is* Low *iff* control == 0

is secure (only) because temp not readable

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since control is not writable, its value now is unchanged from when buffer was read

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buffer's *classification depends on* control: *is* Low *iff* control == 0

secure because buffer was Low when read, so temp holds Low data

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Dependent Security Logic: Intuition

inspired by Mantel et al. CSF 2011

buffer's *classification depends on* control: *is* Low *iff* control == 0

```
skip   /* control +=_m AsmNoW */;
skip   /* temp +=_m AsmNoRW */;
temp := buffer;
if control == 0 then
  low-var := temp
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endif;
temp := 0;
skip   /* temp -=_m AsmNoRW */
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temp is now guaranteed Low

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allow others to read temp: secure (only) because temp guaranteed Low

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buffer's classification depends on control: is Low iff control == 0
temp is classified statically Low

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Type System: Stability and Rewriting

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Type System: Stability and Rewriting

[t : {c=0}] ({c},{t}) {c=0}

Γ $\mathcal{S}$ P

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would make this type meaningless

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i.e. under *P*, its type is equivalent to {}, which doesn't mention control

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Solution: allow types to be rewritten to equivalent ones under *P*

Type System: Stability and Rewriting

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Γ $\mathcal{S}$ P

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Type System: Stability and Rewriting

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                                  skip   /* control +=_m AsmNoW */;
                                  skip   /* temp +=_m AsmNoRW */;
                                  temp := buffer;
                                  if control == 0 then
[t : {}]  ({c},{t})  {c=0}        skip   /* control -=_m AsmNoW */
                                    low-var := temp
                                  else
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Γ $\mathcal{S}$ P

Solution: allow types to be rewritten to equivalent ones under P

Type System: Stability and Rewriting

[t : {}] ({},{t}) {}

Γ $\mathcal{S}$ P

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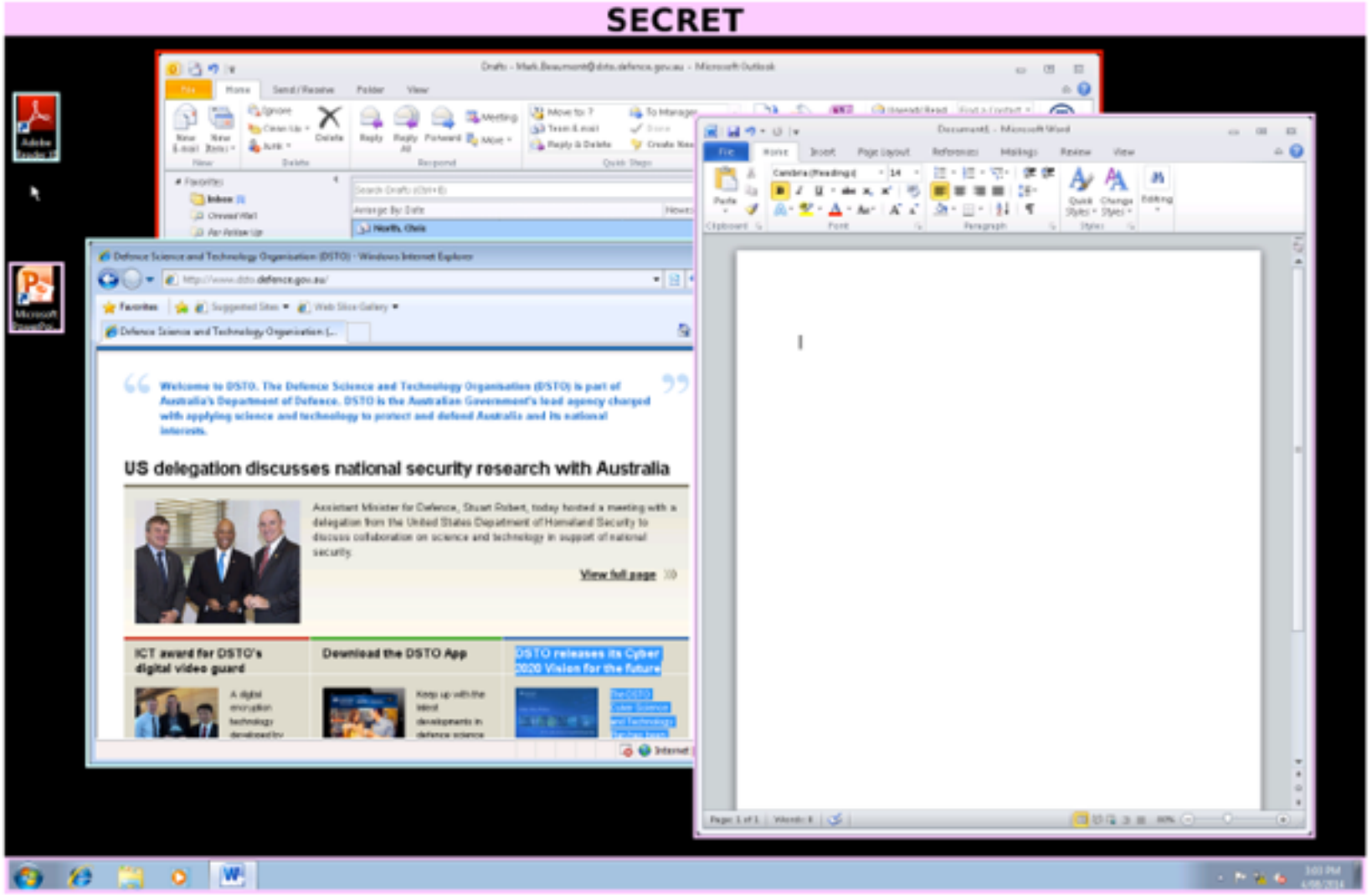
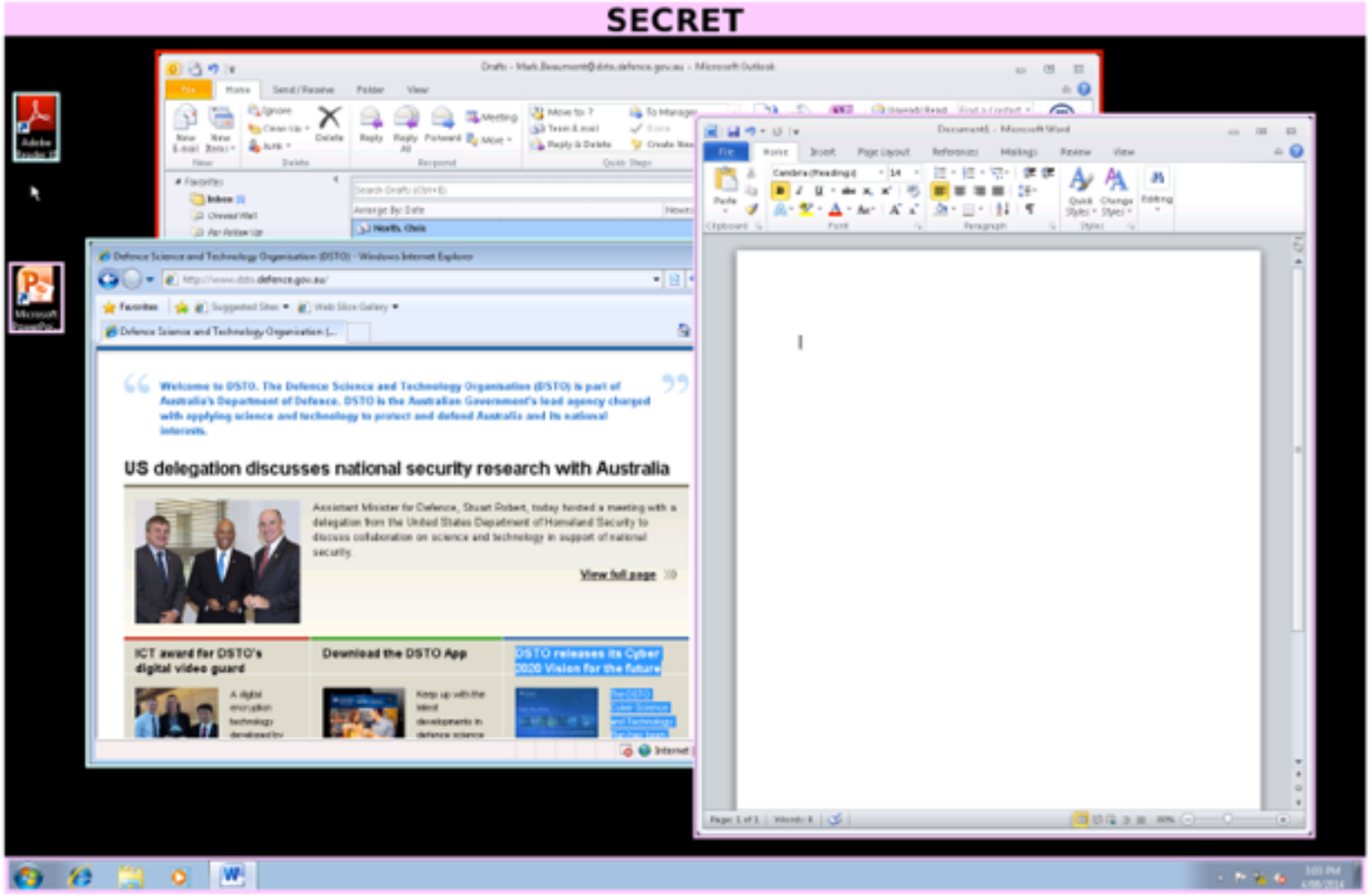
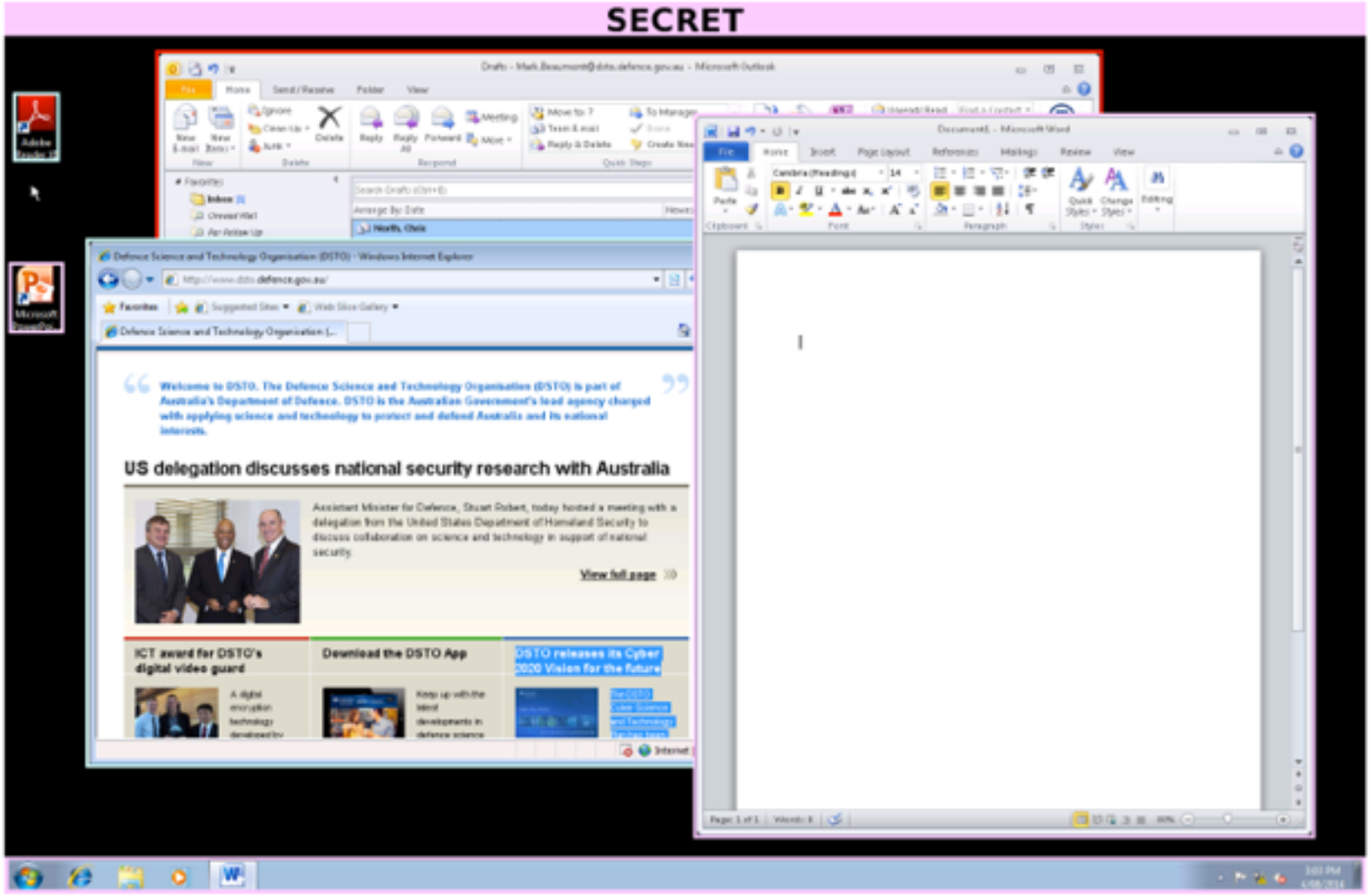
Display Composition: Untrusted Geometry



Dis[redacted]omposition: Untrusted Geometry



Dis  mposition: Untrusted Geometry



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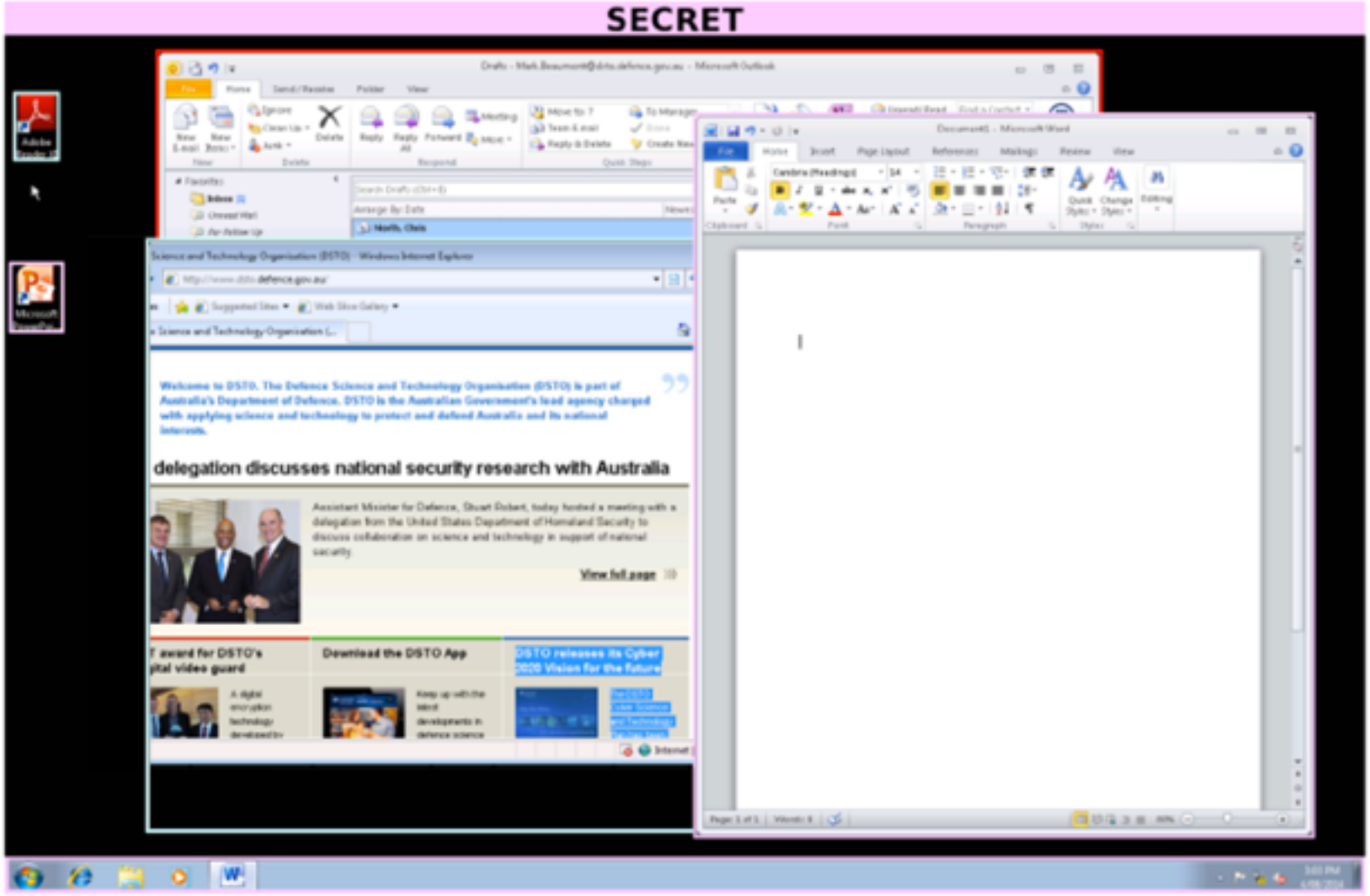

Formalisation

In Isabelle/HOL, available on Archive of Formal Proofs: http://isa-afp.org

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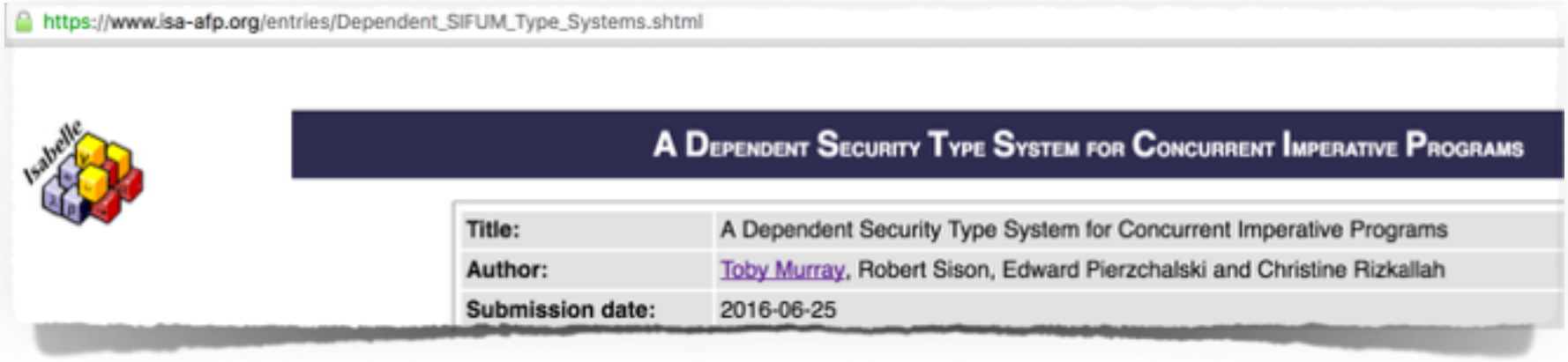
Compositional Security Property and Program Logic:



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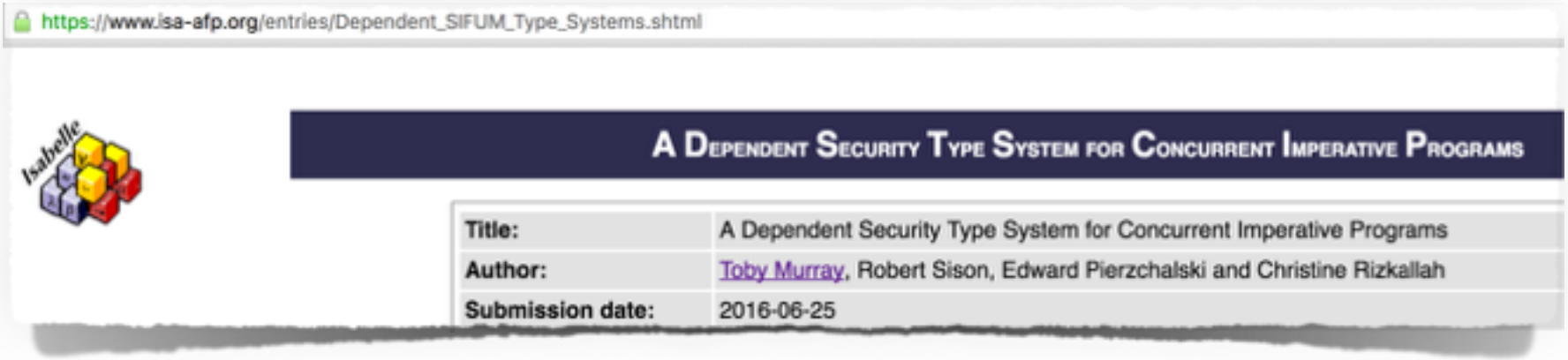
Compositional Security Property and Program Logic:



Compositional Theory of Security Preserving Refinement: